High-Performance III-V Quantum-Dot Lasers Monolithically Grown on Si and Ge Substrates for Si Photonics

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I, Ting Wang, confirm that the work presented in this thesis is my own. Where information has been derived from other resources, I confirm that this has been indicated in the thesis.

Abstract

Self-assembled III-V quantum dots (QDs) attract intense research interest and effort due to their unique physical properties arising from the three-dimensional confinement of carriers and discrete density of states. Semiconductor III-V QD laser structures exhibit dramatically improved device performance in comparison with their quantum well (QW) counterparts, notably their ultra low threshold current density, less sensitivity to defects and outstanding thermal stability. Therefore, integrating a high-quality QD laser structure onto silicon-based platform could potentially constitute a hybrid technology for the realization of optical inter-chip communications. This thesis is devoted to the development of high-performance InAs/GaAs QD lasers directly grown on silicon substrates and germanium substrates for silicon photonics.

In the integration of III-V on silicon, direct GaAs heteroepitaxy on silicon is extremely challenging due to the substantial lattice and thermal expansion mismatch between GaAs and Si. The inherent high-density propagating dislocations can degrade the performance of III-V based lasers on silicon substrates. To enhance the device performance, QW dislocation filters are used here to create a strain field, which bends the propagating dislocations back towards the substrate. Here, we report the first operation of an electrically-pumped 1.3-μm InAs/GaAs QD laser

epitaxially grown on Si (100) substrate. A threshold current density of 725 A/cm^2 and an output power of 26 mW has been achieved for broad-area lasers with as-cleaved facets at room temperature.

To avoid the formation of high-density threading dislocations (TDs), an alternative to direct growth of GaAs on silicon substrate is to use an intermediate material, which has a similar lattice constant to GaAs with fewer defects. Germanium appears to be the ideal candidate for a virtual substrate for GaAs growth, because germanium is almost lattice-matched to GaAs (only 0.08% mismatch). In the last 20 years, the fabrication of germanium-on-silicon (Ge/Si) virtual substrates has been intensely investigated with the demonstration of high-quality Ge/Si virtual substrates. The main challenge for the growth of GaAs on Ge/Si virtual substrate is to avoid the formation of anti-phase domains due to the polar/non-polar interface between GaAs and germanium. A new growth technique was invented for suppressing the formation of anti-phase domains for the growth of GaAs on germanium substrates at UCL. Based on this technique, lasing at a wavelength of 1305nm with a threshold current density of 55.2A/cm^2 was observed for InAs/GaAs QD laser grown on germanium substrate under continuous-wave current drive at room temperature. The results suggest that long-wavelength InAs/GaAs QD lasers on silicon substrates can be realized by epitaxial growth on Ge/Si substrates.

Studies in this thesis are an essential step towards the monolithic integration of long-wavelength InAs/GaAs QD lasers on a silicon substrate, as well as the integration of other III-V devices through fabricating III-V devices on silicon substrates.

List of Publications

Journal Publications:

[1] T. Wang, A. Lee, F. Tutu, A. Seeds, H. Liu, Q. Jiang, K. Groom, and R. Hogg, The effect of growth temperature of GaAs nucleation layer on InAs/GaAs quantum dots monolithically grown on Ge substrates, Appl. Phys.Lett. 100, 052113(2012).

[2] I. C. Sandall, J. S. Ng, J. P. David, C. H. Tan, T. Wang and H. Liu, 1300 nm wavelength InAs quantum dot photodetector grown on Si, Opt. Express 20(10), 10446 (2012).

[3] F. K. Tutu,I. R. Sellers, M. G. Peinado, S. M. Willis, A. R. Watt, T. Wang, and H. Y. Liu, Improved performance of multilayer InAs/GaAs quantum-dot solar cells using a high-growth-temperature GaAs spacer layer, J.Appl. Phys. 111, 046101 (2012).

[4] T. Wang, H. Liu, A. Lee, F. Pozzi, and A. Seeds, 1.3-μm InAs/GaAs quantum-dot lasers monolithically grown on Si substrates, Opt. Express 19, 11381(2011).

[5] H. Liu, T. Wang, Q. Jiang, R. Hogg, F. Tutu, F. Pozzi, and A. Seeds, Long-wavelength InAs/GaAs quantum-dot laser diode monolithically grown on Ge substrate, Nature Photon. 5, 416 (2011).

Conference and Symposia Publications:

[1] T. Wang, A. Lee, F. Tutu, A. Seeds and H. Liu, Optimization of 1.3-μm InAs/GaAs Quantum Dot Lasers on Ge and SiGe Substrates, IOP one-day Quantum Dot Conference (2012).

[2] T. Wang, A. Lee, F. Tutu, F. Liu, F. Pozzi, H. Liu and A. Seeds, Silicon Photonics: InAs Quantum Dot Lasers on Ge/SiGe Substrate, the 8th International Conference on Group IV Photonics (2011).

[3] T. Wang, A. Lee, F. Tutu, A. Seeds and H. Liu, Long-wavelength InAs/GaAs quantum-dot laser diodes monolithically grown on Ge and Si substrates for Si photonics, High-efficiency materials for Photovoltaics (2011).

[4] T. Wang, A. Lee, F. Tutu, F. Pozzi, A. Seeds and H. Liu, Long-wavelength InAs/GaAs quantum-dot laser diodes monolithically grown on Ge substrate, UK Semiconductors Conference (2011).

[5] T. Wang, A. Lee, F. Liu, A. Seeds and H. Liu, 1.3-μm InAs/GaAs quantum-dot laser epitaxially grown on silicon substrate,UK MBE Conference (2011).

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Chapter 1

Introduction

Silicon photonics is the optical analogy to silicon microelectronics, the foundation of the computer revolution. The idea in silicon photonics is to apply the existing fabrication techniques for microelectronic circuitsto a faster data processing medium, light.

Silicon has significant advantages as a substrate over many other semiconducting materials because it is a cheap material with an easy production of oxide, and relatively easy to process. However, there are natural obstacles for silicon to emit and absorb light, which is the minimum requirement for fabricating photonic devices. But fortunately, silicon is transparent for telecom wavelengths, which appears to be an ideal medium for waveguide. In contrast, the systems like GaAs exhibit much smaller effective electron mass than silicon resulting in higher electron mobility, which can produce faster devices. In addition, GaAs-basedmaterials offer a tremendous optical performance and efficiencies.

Therefore, integrating III-V photonic materials and devices ona silicon platform can be the most beneficial combination. There are high-performanceSiGe modulators and photodetectors available, but a silicon-basedlight source has still remained to be the main challenge here to be overcome. While the hybrid III-V/Si lasers by wafer bonding have been extensively studied with the demonstration of high-performance room-temperature lasers at telecom wavelength, but are suffering from a low yield and high cost. In this thesis, we

have made the first 1.3μm quantum dot (QD) laser on both silicon and germanium substrates at room temperature, which can be further developed for monolithic integration.In order to investigate silicon-based III-V QD photonics, the concepts of semiconductor nanostructures and silicon photonics need to be clarified first in this chapter.

1.1 Motivations for Silicon Photonics

As all current existing photonic systems are based on III-V compound semiconductors, the merger with silicon microelectrocnicswould ease the scalability and integration of fabrication for photonic devices. To be a candidate material of photonic device fabrication, the requirements are ease of processing, low fabrication cost and high optical performance. Unfortunately, both III-V compound and group IV semiconductors only meet one or two of these standards. III-V semiconductors have high optical efficiency, but also the difficulties of device processing (poor mechanical properties) and extremely high per-unit cost appear to be the main challenges to photonic engineering in past 5 years. Therefore, III-V photonic devices have hardly been integrated on a large scale, and they are only used in applications where there are no other choices for replacement.

On the other hand, look intothe conventional silicon-based electronic chip industry, which embodies the height of technological sophistication and economics of scale, with the capability of producing complex circuitry, boasting over one billion components at very low cost that appear in everyday electronic products. In this case, silicon appears to be the most promising candidate for lowering the per-unit price of photonic systems, as silicon being the most well established semiconductor for large-scale device fabrication with advantages in both complexity and cost per unit device. Although silicon-based light generation, detection and modulation techniques have been extensively explored, they are still far from practice and limited by the indirect bandgap of silicon[1], the significant challenge posed by nature. In contrast, directbandgapIII-V compounds have robust photonicproperties that can be tailored for III-V emitters and detectors operating atvarious wavelengths with fast light-conversion speeds and sufficient light-power output for many photonic applications. Therefore, integrating III-V photonic components on a silicon platform would be the ideal solution for both high performance and low cost. Over the past twenty years, a huge

amount of epitaxial growth research on III-V on silicon substrate has been carried out. But due to the lattice mismatch between III-V semiconductors and silicon, low-defect-density III-V/Si wafers has not been achieved. In this project, we aim to develop the most advanced growth technique and heterostructurestructures differing from any conventional epitaxial growth for low-defect-density III-V buffer layers on silicon substrate and to develop semiconductor III-V QD lasers on it.

1.1.1 Scientific Background for Silicon Photonics

Starting from 2004, Intel has introduced their silicon photonic devices, but various limitations including cost and complex assembly kept them away from the practical industry. As we all know, silicon is a poor light emitter by nature due to its indirect bandgap, as shown in Figure 1.1 (right).In direct bandgap materials (for example, GaAs and InP) radiative recombination occurs rapidly and efficiently via a simple two-particle process, as shown by the simplified band diagram in Figure 1 (left). Direct bandgap materials have a structure in which the lowest energy points of both the conduction and valence bands line up vertically in the wave vector axis, which means that they share the same crystal momentum. This is the principal reason why GaAs- andInP-based materials have been the dominant material systems for semiconductor diode lasers since their first demonstration in 1962. In a direct band structure (such as InP in Figure 1.1), electron–hole recombination almost always results in photon emission, whereas in an indirect band structure (such as Si in Figure 1.1), free-carrier absorption, Auger recombination and indirect recombination exist simultaneously, resulting in little photon emission.

Si and Ge areindirect bandgap materials, and are not naturally capable of accomplishing efficient radiative recombination. Free electrons tend to reside in the X valley of the conduction band, which is not aligned with free holes in the valence band (Figure 1, right). Therefore if a recombination is to lead to emission of a photon, a third particle must be involved to carry away the excess momentum, which results in slow optical transition rates. A major non-radiative process is Auger recombination, in which an electron (or hole) is excited to a higher energy level by absorbing the released energy from an electron–hole recombination. The Auger recombination rate increases with injected free-carrier density

and is inversely proportional to the bandgap. Free-carrier absorption (FCA) represents another major non-radiative process wherein the free electrons in the conduction band can jump to higher energy levels by absorbing photons. In high-level carrier injection devices (lasers and amplifiers, for example) or heavily doped layers, free-carrier loss is orders of magnitudes higher than the material gain. For both Auger recombination and FCA, the electrons pumped to higher energy levels release their energy through phonons, rather than by emitting photons. Consequently, semiconductor laser research over the past fifty years has primarily focused on compound semiconductor substrates, but now there is intense interest in lasers on Si, such as Intel. The most recent demonstration of a continuous wave all-silicon laser is Raman Effect based device[3]. But the Raman laser is optically pumped, which makes chip-level integration impractical[1].

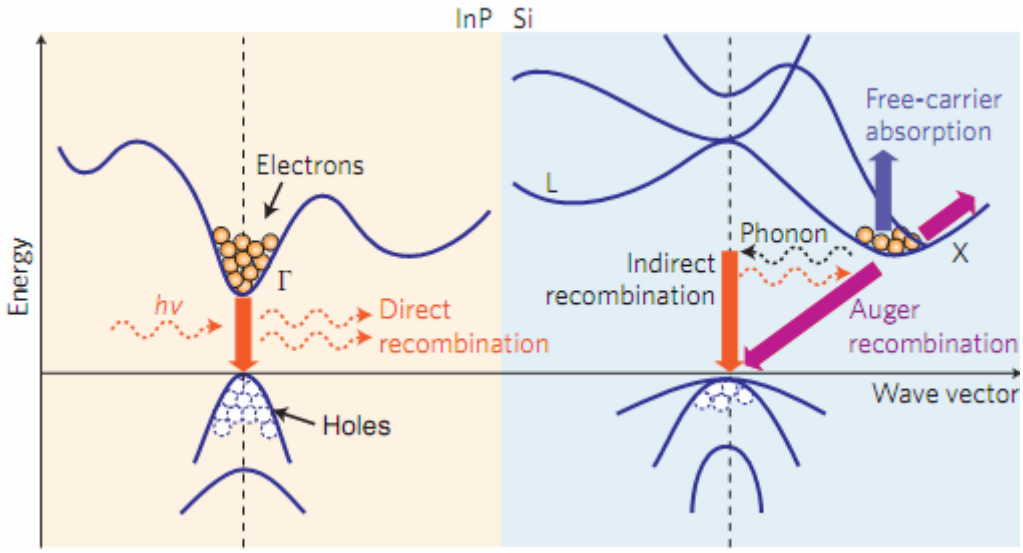

Figure 1.1: Energy band diagrams and major carrier transition processesin InP and crystalline Si.

Unlike silicon, III-V compound semiconductor can be used to produce extremely high efficiency light emitting devices. Conventional III-Vquantum well (QW) lasers grown directly on silicon substrate are characterised by short life time, due to large defect densities within the active region caused by dislocation propagation from the interface between GaAs buffer layer and Si substrate. The dislocation at the GaAs/Si interface is caused by the 4% lattice mismatch, non-polar/polar interface and 250% thermal expansion difference betweenGaAs and silicon[2]. There are currently many existing III-V heterostructures on different materials

designed for highly efficient laser emission. To select a silicon compatible III-V heterostructure for communication purpose, the proper buffer material and emission material play an important role. The list in Table 1.1 contains relevant physical properties of possible choices of III-V compound materials on silicon at room temperature. Most III-V compound semiconductors have a large lattice mismatch and thermal expansion coefficient compared with silicon, which indicates the likelihood of high defect densities of III-V/Si epitaxial structures. To overcome this obstacle, various techniques should be investigated to achieve III-V/Si compatibility.

Physical Properties at 300K/Materials	Silicon	Germanium	GaAs	InAs	GaP	InP	GaSb	AlSb	InSb
Band Gap Energy(0.8 eV = 1.55um)eV	1.12 (Indirect)	0.661 (Indirect)	1.424	0.354	2.26 (Indirect)	1.344	0.726	1.6(Indi)	0.17
Lattice Constant(A)	5.431	5.658	5.65325	6.0583	5.4505	5.8687	6.09593	6.135	6.479
Electron Mobility(cm2/V/s)	1400	3900	8500	40000	250	5400	3000	200	77000
Hole Mobility(cm2/V/s)	450	1900	400	500	150	200	1000	400	850
Melting Point(°C)	1412	937	1240	942	1457	1060	712	1080	527
Thermal Conductivity(W cm-1°C 1)	1.3	0.58	0.55	0.27	1.1	0.68	0.32	N/A	0.18
Thermal Expansion Coefficient(10-6°C -1)	2.6	5.9	5.73	4.52	4.65	4.6	7.75	N/A	5.37
Infrared Refractive Index	3.42	4	3.3	3.51	3.02	3.1	3.8	3.3	4
Surface microhardness(kg/mm2)	1150	780	750	430	850	460	450	413	220

Table1.1: Physical Properties of III-V compound semiconductor materials at 300K.

1.1.2 Obstacles toDirect Growth of III-V Compounds on Silicon

GaAs-based electronic and photonic heterostructures have been wellexplored in the past decade. If there are so many technical obstacles with GaAs-on-Si (GaAs/Si) technology, why don't we stick to GaAs substrate as an alternative choice? The answer is the mechanical frigidity and poor thermal conductivity of GaAs substrate, which make chip-level integration harder. Additionally, GaAs substrates are relatively expensive and have inferior mechanical properties than silicon substrate. As mentioned above, due to the lattice mismatch and thermal expansion difference, strain induced dislocations are generated at the GaAs/Si interface. Furthermore, the growth of a GaAs epitaxial layer on Si would have dislocations propagating along the growth direction; even reaching the active region of the emitting device. Therefore, current research focuses on the reduction of these strain-induced thread dislocations (TDs). The other type of defects degrade the material quality are anti-phase domains (APDs), which are generated from the nature of atomic polarity difference between Si and GaAs, where GaAs has a polar atomic structure, while Si was non-polar.

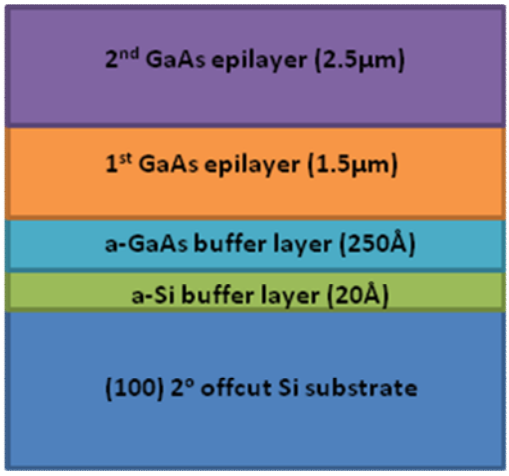

Figure 1.2: Schematics of Si/GaAs double buffer layers[4].

One of the initial ideas is to grow a thick amorphous GaAs at a low growth temperature over the silicon substrate as a buffer layer, but the reduction of defects is relatively low for this technique. An improvement is possible with Si and GaAs double buffer layers as shown in Figure 1.2. It is verified that the PL intensity of the GaAs emission is nearly doubled, and the linewidth is narrowed for better wavelength resolution[4]. From the

TEM image in Figure 1.3, we could observe that the dislocations are dramatically reduced in the double buffer layer, which offers a better-quality and lower cost GaAs/Siepi-layer growth.

But this technique suffers from contamination induced by two-step growth of a-Si (amorphous Si) and a-GaAs (amorphous GaAs). Therefore, there is a much more effective buffer structure, such as QW dislocation filter, which has been demonstrated in Ref. 6 for the purpose of achieving highly efficient and long lifetime photonic device.

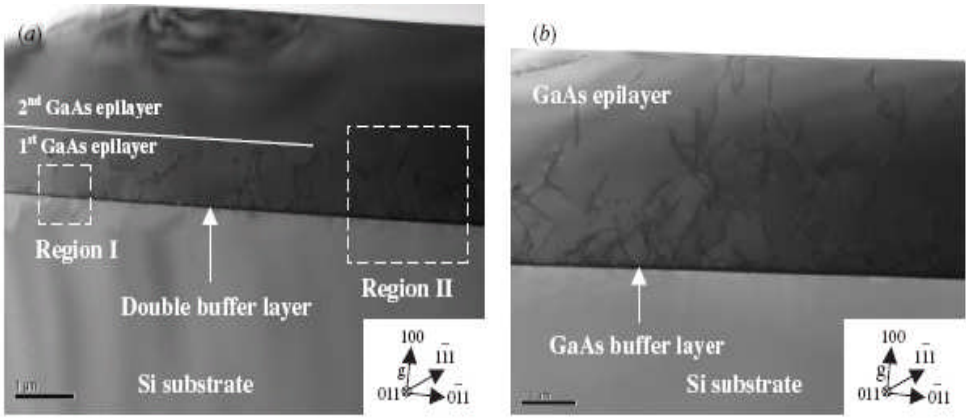

Figure 1.3: TEM cross-sectional images of GaAs/Si double buffer layer and GaAs single buffer layer on Si substrate[5].

1.1.3 Quantum-Well Dislocation Filter

The most typical semiconductor laserare fabricated onGaAs and InP substrates. Recent research activities have brought a high-quality dislocation filter to reduce the propagation of the defects generated at the GaAs/Si interface to the active region as shown in Figure 1.4. TheInGaAs QWs on GaAs generates a strain field induced by lattice mismatch at the InGaAs/GaAs interface[7]. The strain field prevents the dislocation from GaAs/Si interface propagating further to the device. The bending of this dislocation will generate a segment of a misfit dislocation, which glides below theInGaAs layer. Bending will occur when the strain energy is released due to generation of the misfit dislocation. Apparently, large lattice mismatch between InGaAs and GaAsis most suitable for dislocation filters. But excessive strain may induce additional dislocations at the interface. Therefore, a relatively low composition of indium (15%) in InGaAs QWs should be used here for an intermediate strain

field. In the case of multiple strained-layer superlattice, it is expected that a multiple QW layer stack will be a more efficient dislocation filter and will enhance the bending of propagating dislocations. The repeated growth of this heterostructure would reduce the dislocation density at the active region as much as possible, and hence, produce a QD laser with high efficiency and long lifetime[9].

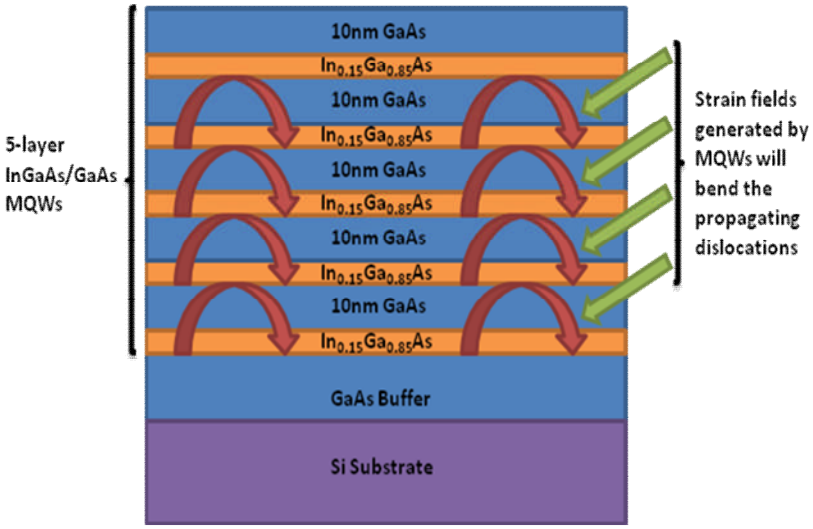

Figure 1.4: Schematic of InGaAs/GaAsmultiple QW dislocation filter grown on Si substrate.

On the other hand, a SiGe/Sivirtual substrate can also be used to grow a high-quality GaAsepilayer, because Ge and GaAs have similar lattice constants and thermal expansion coefficients. However, one of the problems is how to grow a high quality Ge layer on the top of the Si substrate, as Ge has 4.2% lattice mismatch to Si. Fortunately, several mature technologies to produce low-defect-densitySiGe substrates, such as composition-graded SiGe substrate [11]or Ge-on-insulator (GeOI) on silicon[12], have been developed in the past decade. For example, the index-gradedSiGe virtual substrate consists of three layers, which are $Si_{0.1}Ge_{0.9}$, $Si_{0.05}Ge_{0.95}$ and Ge layers as shown in Figure 1.5. A large number of non-propagating and closed-loop dislocations is formed at the $Si_{0.1}Ge_{0.9}$/Si interface due to their large lattice mismatch. The rest of the upward propagating dislocations are deflected or bent by the strain fields induced by misfit dislocations at the $Si_{0.1}Ge_{0.9}$/ $Si_{0.05}Ge_{0.95}$ interface and the $Si_{0.05}Ge_{0.95}$/Ge interface[10]. In this case, a very low density of threading dislocation can propagate into the Ge layer. Therefore, we can subsequently grow a high quality InGaAs/GaAs dislocation filter on top of this virtual substrate for further reducingthe

threading dislocation density. Apart from its outstanding performance at dislocation filtering, one of themajor challenges in the growth process of SiGe buffer layer is the carry over Ge from the initial Ge growth into subsequent III-V semiconductor layer, called a memory effect of Ge epitaxial growth. The reason for it is the contamination of germanium on the reactor wall and diffusion within the structure.

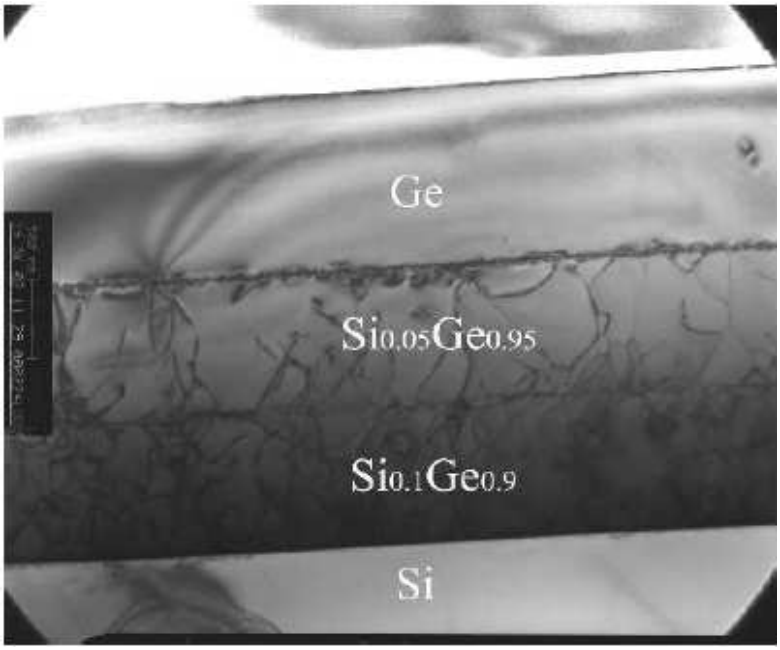

Figure 1.5: TEM image of SiGe buffer layers[11].

So far, theInGaAs/GaAs QWdislocation filter is the most promising candidate to produce III-V on silicon optoelectronic devices in comparison with other existing methods. Therefore, the incorporation of QW dislocation filter and GeSi/Si virtual substrate appears to be the most ideal combination of creating a high-performance III-V/IV hybrid photonic device.

1.1.4 Adhesive Bonding Method

InP-based devices have been the most reliable technology in applications at telecom wavelength, because they support both light generation and detection in the telecom wavelength windows from 1.3 to 1.55µm, where the dispersion and attenuation properties of optical fibres are minimum. There are many existing functions which can be performed on InP based devices: optical amplification, modulation, switching, and so on. Benefiting

from its physical property, the InP-on-silicon (InP/Si) integration would be a straight solution to low-cost commercial photonic chips. Unfortunately, as mentioned above, the extremely large lattice mismatch and thermal expansion difference between InP and Si prevent direct growth of InP structures on silicon. Therefore, the attention has come to direct bonding InP based light-emitting device to the silicon substrate, as shown in Figure 1.6[12].

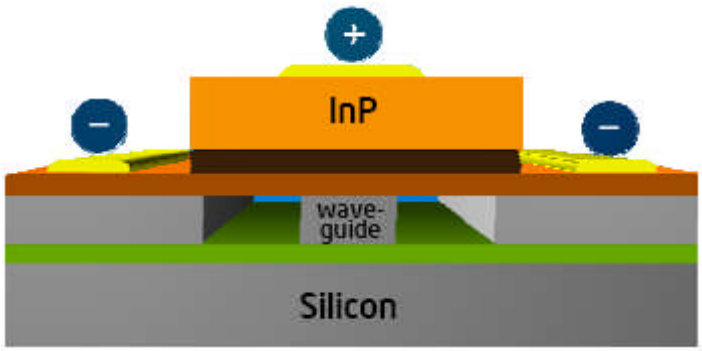

Figure 1.6: Schematic of InP laser bonding to silicon substrate.

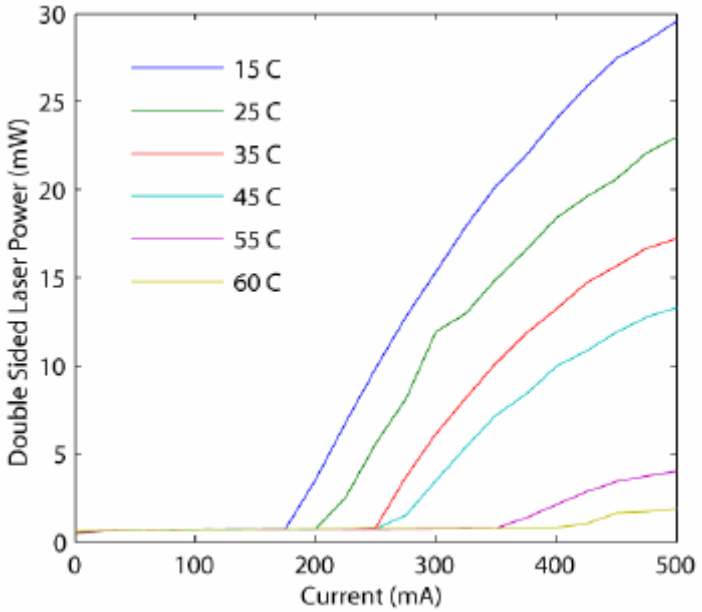

Figure 1.7: Continuous-wave power versus current characteristics.

On September 18, 2006, Intel and the University of California, Santa Barbara (UCSB) announced the demonstration of the world's first electrically driven hybrid silicon laser, which is based on this bonding method [12]. It brings the InP light-emitting device to the ultra flat silicon wafer with the existence of an oxide thin layer in the middle, acting as a

'glass glue', where the production of the oxide layer is plasma assisted. When it is heated up, the InP emitter and Si wafer are simply fused together. While a voltage is applied across the InP emitter, electrons and holes recombine in the middle and generate a laser beam emission at 1.31 or 1.55 µm. Underneath the oxide thin layer, silicon acts a waveguide due to its transparency at infrared wavelengths. While theInP laser generates the light beam, it will be directly coupled into the silicon waveguide, and hence creates a hybrid silicon laser by adhesive bonding. This approach offers the possibility of future low cost and high performance photonic circuit integration. But there are also existing challenges, which are the low thermal conductivity of the oxide bonding layer. At room temperature, the lasing behaviour of InP dies after a temperature increment up to 60 ^{o}C as shown in Figure 1.7[12]. In addition, the coupling efficiency of InP generated laser beam into Si waveguide is highly dependent on the thickness of the bonding layer, which may cause unwanted high resistance to appear. To commercialise this technique, there are still many challenges expecting to be solved, including the poor thermal conductivities, coupling efficiency and low production yield.

1.2 Advantages of Quantum-Dot Devices in III-V/Si Integration

The advantages of quantum-dot lasers were predicted in the early 1980s, based on the atomic-like, discrete density of states. An ideal QD laser exhibits a significantly lower threshold current density (J_{th}) in comparison with traditional semiconductor quantum well (QW) lasers and a temperature insensitive operation. Since the initial report of self-assembled QD lasers, despite relatively large inhomogeneous linewidths, significant progress has been made with best reported room-temperature J_{th} of 12A/cm^2 [12], which is a factor of four less than comparable quantum-well laser values (~50 A/cm^2), and temperature-independent operation between -20 and 85^{o}C[13]. These special QD laser's advantages (a lower power consumption and more stable operation) promote the initiatives to develop III-V QD devices on Si. Furthermore, QD structures offer several other special advantages, not directly related to their unique density of states, over quantum wells to produce better III-V/Si emitters, including the low sensitivity to defects and the high resistance to degradation.

1.2.1 Lower Sensitivity to Defects

Some of the threading dislocations generated at the III-V/Si interface will propagate through the III-V layers. Every threading dislocation propagating through QWs will becomea non-radiative recombination centre, and hence degrade whole device performance.With relatively high threading dislocation density in the active region, the performance of III-V/Si QW devices will degrade dramatically. However, in the case of QD devices, one threading dislocation in active region can only "kill" one or a few dots. It will not affect the majority of dots. Furthermore, the electrons and holes within active region are spatially localised in dots. This carrier localization could result in carriers not "seeing" the threading dislocations. QD devices thus exhibit dramatically reduced sensitivity to the defects, which makes it much easier to realise higher-performance III-V QD lasersepitaxially grown on Si substrate.

1.2.2 High Resistance to Degradation

The strain field of QDs gives greater mechanical strength to prevent the movement of dislocations, even in the presence of high-density non-radiative recombination centres[13]. It is well established that defects attract higher current densities during the operation of semiconductor laser diodes, leading to the movement and growth of defects and hence rapid device failure in QW laser diodes[5]. Therefore, in the case of III-V/Si devices with relative high threading dislocation density (TDD), QD lasers should exhibit much longer lifetime than that of QW devices, as one TD can only kill one or a few dots. These advantageous properties lead to recent demonstration of III-V/Si QD lasing up to 95 ^{o}Cat 1.1 μm with room-temperatureJ_{th} of ~900 A/cm^{2}which is significantly better than those of III-V/Si QW lasers[8]. Further major studies on developing high-quality III-V/Si QD lasers at communication wavelengths with low room-temperature J_{th} is critical for integrating III-V photonic components into Si electrical circuits.

1.3 Low Dimensional Semiconductor Structures

Low dimensional semiconductor structures are nanometre-scale semiconductors, which can provide carrier confinement in more than one direction. As shown in Figure 1.8,

each reduction in dimensionality leads to unique physical characteristics. A quantity which is crucial in quantum mechanics for the properties of particles is their density of states. A semiconductor QW is a two-dimensional structure, as carriers can move freely in two directions, with only one-dimensional confinement. Similarly, a quantum wire is a one-dimensional structure having carrier confinement in two directions. Ultimately, the ideal case would be a zero-dimensional structure, i.e. quantum dot, which can obtain all-direction carrier confinement and generate discrete energy states.

The benefits of achieving three-dimensional quantum confinement in semiconductors have been predicted since last century, but it is only recently that defect-free quantum-dot devices have been realized with reproducible structural, electronic and optical properties.

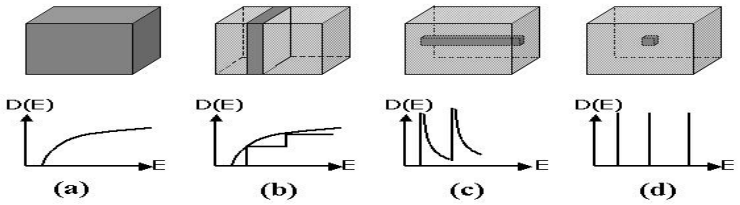

Figure 1.8: Density of states in semiconductors of decreasing dimensionality, from a) bulk(3D) to b) 2D (quantum well) to c)1D (quantum wire) to d) 0D (quantum dot).[19]

1.4 Quantum Confinement in Semiconductor Nano-structures

As discussed above, the interest in semiconductor nanostructures mainly arises because they allow the nature of the electronic energy levels to be modified. Both the form of these levels and how they are distributed energetically (their density of states) can be changed in useful ways. In addition, the optical path of generated light can be confined by specially designed semiconductor heterostructure in a similar way.

1.4.1 Quantum Confinement in a Quantum Well

In a bulk semiconductor, electrons and holes are free to move in all directions, which indicate the loss of energy. However, the restriction of motion to 2 dimensions is possible, if we make a very thin semiconductor sheet restricted in a third direction, perpendicular to the plane. Such a system is known as a quantum well.

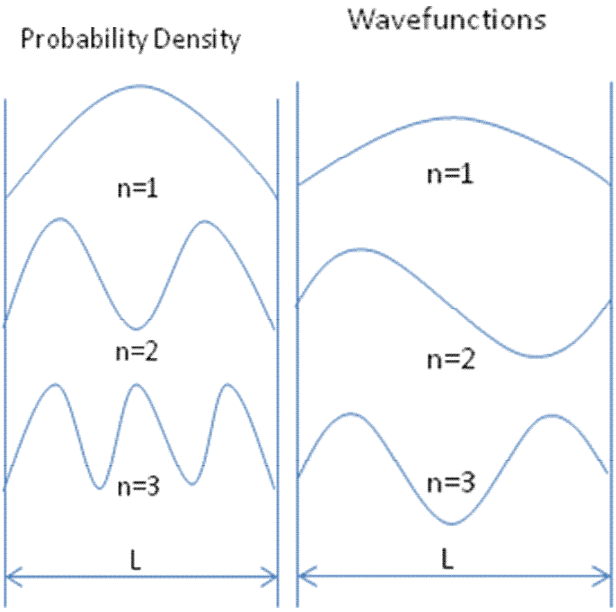

Figure 1.9: Particle in a box.

In a quantum well, electrons and holes are trapped in one dimension, called particle-in-a-box (Figure 1.9). For motion parallel to the plane of sheet, the wavelength of particles must be such that the amplitude of the wave is zero at the edge of the well. This phenomenon is identical to the allowed vibrational modes of a stretched string which is fixed at each end [20]. The first 3 allowed modes are shown in Figure 1.9.

For the topmost mode, which is the lowest allowed energy level (n=1), one half of the wavelength fits into the width of the well. The corresponding probability density shows that this particle is most likely to be found in the middle of the well for the lowest allowed mode. Similarly, we have second order mode (n=2) that equals the width of the quantum well, and 3/2 wavelength for the third order mode. In comparison, the probability distributed second order mode has the particle forbidden in the middle of the well. All these lead to a general result: the only allowed wavelengths or energy states are those such that an integer number

of half wavelengths lie within the well width L. In the ideal case, the height of the quantum well is always infinite.If not, there is possibility of barrier penetration. In this case, a certain probability of finding the particle beyond the barrier will appear[20]. Thus in practice, we would always like to have a well as deep as possible to optimise the carrier confinement.

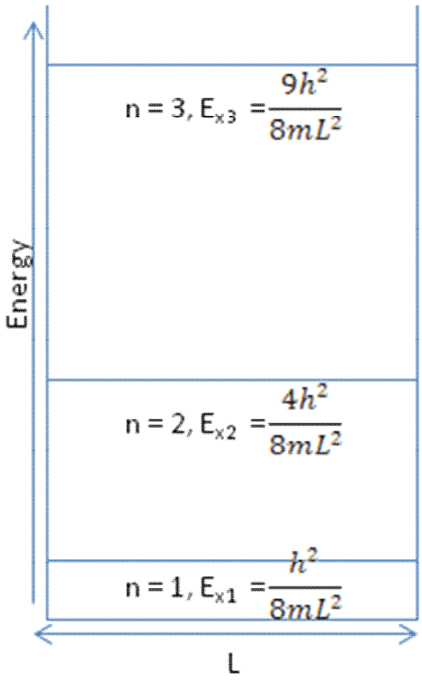

Figure 1.10: The first three quantised energy levels for a quantum well

The energy (E) corresponding to motion in to the plane can be written in the following equation:

$$= \frac{h^2}{2\ ^2} = \frac{h^2\ ^2}{8\ ^2}$$

where λ is the de Broglie wavelength, h is Planck's constant , n is the quantum number (n = 1, 2, 3, 4...), and L is the width of the well.

This equation gives the discrete allowed energy levels depending on the quantum number n. Thus, the discrete energy of particle is said to be quantized. In the case of quantum well, the quantization only occurs for motion in the plane of the sheet (x direction). Motion within the plane is free to move in the other two directions, and not quantized. Figure 1.10 shows the first three quantized energy state of a quantum well. Note that because the energy level depends upon the quantum number n, spacing between neighbouring energy levels become more separated as n increases.

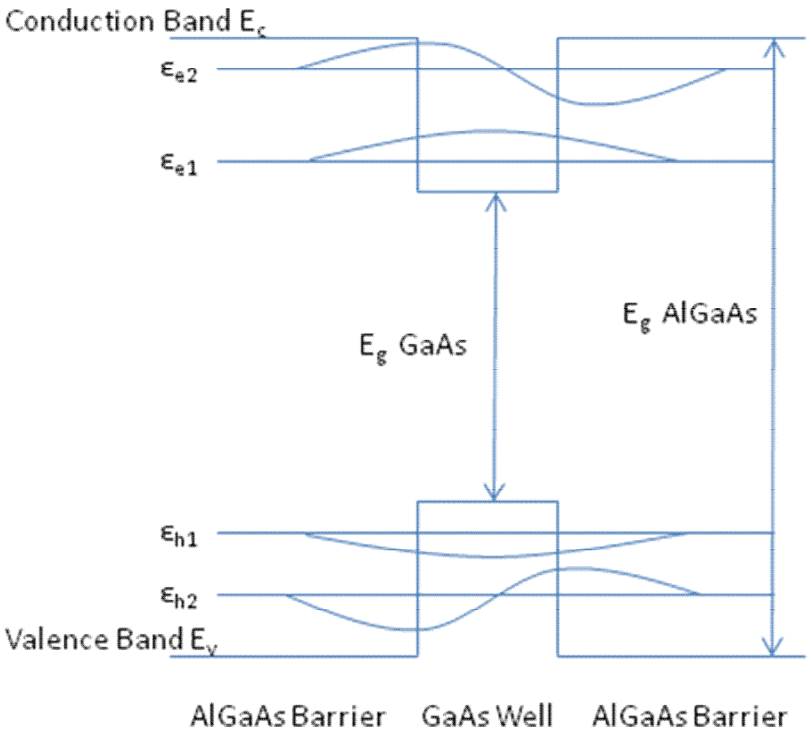

Figure 1.11: The valence and conduction band potential wells and confined wavefunctions of a semiconductor quantum well.

In the ideal case of an infinitely deep potential well, there are an infinite number of quantized energy states. In practice, a quantum well has a finite depth and is formed by placing a thin layer of one semiconductor between two thicker layers of a second semiconductor, which has a larger bandgap, to form a sandwich structure (Figure 1.11). Within this structure, a potential well of finite depth results in a quantization of both the electron and hole energies for motion normal to the plane of the well.

In addition, there is no longer an infinite number of quantised levels, the precise number depends upon the depth and width of the well. However in many cases the energy levels in a finite depth quantum well, particularly the ground state energy, can be calculated with reasonably accuracy by assuming an infinitely depth well. The form of conduction and valence bands for a quantum well and the wavefunctions of the quantised electron and hole levels are shown in Figure 1.11.

Once incident light enters the quantum well structure, it excites one of the electrons at lowest energy level of valence band into conduction band. Then the excited electron in conduction band would recombine with a hole at ground energy state of valence band in

the intrinsic region, therefore, producing a photon. By the same principle, free electrons can be produced without light excitation by injecting carriers.

The quantum-well heterostructure is normally doped to be a p-n junction. By applying a forward bias to it, the energy potential can diffuse injected electrons and holes into the quantum well, where is the intrinsic region of this p-n junction. The injected electrons would thus recombine with injected holes, producing sufficient amount of photons. The energy of photons produced is simply the bandgap of the semiconductor. For a quantum well the photon will have an additional energy given by the energy difference between ground energy states and band edges of conduction and valence band [20].

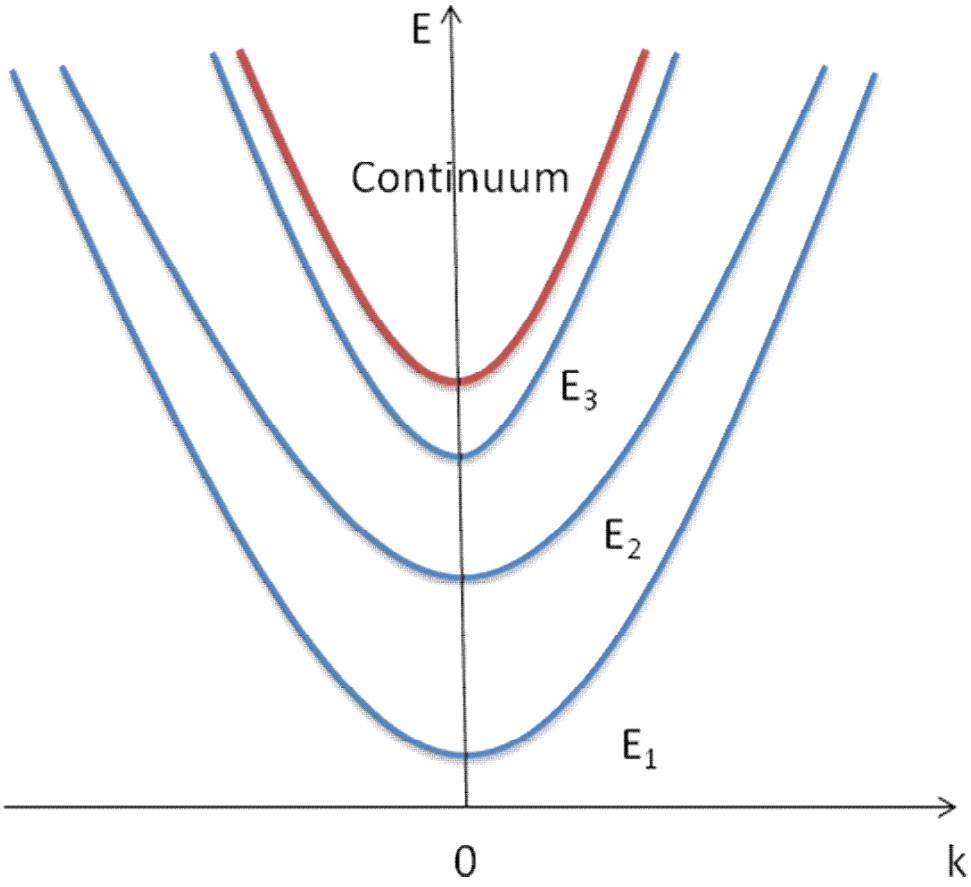

Figure 1.12: Confined quantum well levels with inplane dispersion.

Using the result for an infinite depth well for these energies, the effective quantum well bandgap can be evaluated:

$$= + \frac{h^2}{8 \cdot 2} + \frac{h^2}{8 \; _h^{\cdot} \; ^2}$$

whereE_g is the bandgap of the bulk semiconductor from which well is made of and and correspond to the electron and hole effective masses.

Furthermore, as electrons and holes are free to move in the plane of a quantum well, a continuous energy band can be formed due to motion in the plane of the well and added to the discrete energy resulting from confinement normal to the plane. As shown in Figure 1.12, the continuous in-plane energy tends to blur the discrete levels from quantisation, thus, forming a continuous energy band.

1.4.2 Advantages of Quantum Dots

The ultimate quantum confinement is provided by an artificial atom called a quantum dot, which consists of a small block of semiconductor surrounded by a second larger bandgap semiconductor. By employing quantum dots, carrier motion is quantised in all three dimensions. If a quantum dot has spatial sizes L_x, L_y and L_z, the total quantisation energy can be written in the sum of three separate terms:

$$,, = \frac{\hbar^2 \; 2}{0 - 2} + \frac{\hbar^2 \; 2}{0 - 2} + \frac{\hbar^2 \; 2}{0 - 2}$$

where (n,m,l) = 1,2,3,4…

At last, the quantisation energy is a function of three quantum numbers n, m and l. Because all motion is quantised in three dimensions, there is no continuous energy term in a quantum dot. Hence, all energy levels within a quantum dot are separated and discrete in ideal cases. The discrete nature of the density of states also reduces the thermal spread of carriers within their bands. Both these aspects are expected to reduce the threshold current density of laser diodes and increase their quantum efficiency. As the photoluminescence of quantum dots is relatively weak, additional multiple quantum wells can be occupied to improve the optical performance of quantum dots, called dots in a well (DWELL). The gain can be improved by a factor of number of DWELL in this structure.

In conventional QW lasers, threading dislocations (TDs) tend to propagate into QW layers in the active region, generating a large non-recombination centre, which can destroy the entire active region. Different from QW-based photonic devices, QD-based devices are less sensitive to defects. TDs can only destroy one QD or a few QDs, while the rest remain optically active. In addition, QD lasers have low threshold current density and are less

temperature sensitive in comparison with QW lasers. As there is enormous strain and defects generation occurring on III-V/IV epitaxial growth, QD-based device appear to be the ideal candidate here. Further details will be discussed in Chapter 2.

1.5 Semiconductor Lasers

The optical confinement of low-dimensional semiconductors has been extensively discussed above. Therefore, it should be no surprise to find that there are many applications of low-dimensional structures in optoelectronic devices. The semiconductor laser has become the most common form of laser, as it can be operated at different wavelengths by employing different semiconductor compounds, which leads to a variation of bandgap and requires only electrical power. Because of its compact size and capability for high-frequency modulation, the semiconductor laser is one of the most important light sources for optical fiber communication. In this case, the incorporation of low-dimensional semiconductor structures enables the route to ultra-high speed global data transfer.

The first optical fibres were designed to operate in the wavelength range of around 800-900nm. As shown in Table 1.2, GaAs and AlGaAs structures were the most appropriate materials for the development of lasers and LEDs in this first operating window. Soon after physicists realised that the minimum intra-modal dispersion appears at 1310nm [22], the second operating window is defined to be 1300nm. By the same time, the operating window has been further extended to 1550nm, which provides low attenuation. Nowadays, both 1300nm and 1550nm wavelengths are used separately for semiconductor lasers for short haul and long haul applications [21].

In order to operate at 1550nm, an optical source can be produced by modification of the composition of the material developed for 1300nm. By using GaAs technology (most mature and reliable technique), the emitting wavelengths between 800-1100nm can be achieved easily, but lasers and LEDs operating at second window are hard to achieve. Only recently, with the dramatic development of material growth techniques, the emitting wavelength of InGaAs lasers extended to 1310nm by employing InAs quantum dots as active layer.

Active Layer	Confining Layer	Wavelength	Substrate
GaAs	(AlGa)As	800-900nm	GaAs
GaInP	(AlGa)InP	630-650nm	GaAs
InGaAs	GaAs	900-1300nm	GaAs
InGaAs	InGaAsP	1550nm	InP
InGaAsP	InGaAsP	1300-1550nm	InP
InAsP	InGaAsP	1060-1400nm	InP
InGaAs	InP	1550nm	InP

Table 1.2: Material systems and wavelength ranges.

Hence, the development of phosphorus-containing quaternary materials is required to extend the operating wavelength, such as GaInAsP, which has been grown epitaxially on InP substrate. By adjusting the composition of the active-layer material and confining-layer material, the wavelengths can be easily tuned between 1100nm-1600nm to be selected for different applications on InP substrate. Unfortunately, InP has proved to be extremely difficult for device processing and expensive for large-scale integration.

1.5.1 Basic Laser Theory

To form a laser, the concept of an optical cavity has to be defined first. The origin of the optical cavity is simply two mirrors in parallel; therefore, light is bouncing between mirrors forming an optical cavity. But an optical cavity is not sufficient to generate enough optical amplification for the laser action. In this case, population inversion is an essential condition required for light amplification within the cavity. By pumping free electrons to excited energy states, there are more electrons at excited states than the ground state. A non-equilibrium state called population inversion can thus be achieved simultaneously [22]. Light amplification in the laser occurs when a photon colliding with an atom in the excited energy state causes the stimulated emission of a second photon and then both these photons release two more. Continuation of this process effectively creates avalanche multiplication incorporating population inversion. To achieve this, an amplifying medium and optical cavity are both necessary. While the optical signal is bouncing between both ends of the cavity, the structure therefore acts as a Fabry-Perot resonator.

Semiconductor lasers are similar to these Fabry-Perot solid-state and gas lasers in that the emitted radiation has spatial and temporal coherence, and laser radiation is highly monochromatic (of small bandwidth). However, semiconductor lasers differ from other lasers in several important aspects:

1. In conventional lasers, the quantum transitions occur between discrete energy levels, whereas in semiconductor lasers the transitions are associated with the band properties of materials.
2. A semiconductor laser is very compact in size. In addition, because the active region is very narrow, the divergence of the laser beam is considerably larger than in a conventional laser.
3. The spatial and spectral characteristics of a semiconductor laser are strongly influenced by the properties of the junction medium.
4. For a p-n junction laser diode, the lasing action is produced by simply passing a forward current though the diode itself. The result is a very efficient overall system that can be modulated easily by directly modulating the current. Since semiconductor lasers have very short photon lifetimes, directly modulation at high frequency can be achieved.

1.5.2 Threshold Current Density

As mentioned above, population inversion is a necessary condition for lasing action. Only population inversion is not sufficient for lasing to occur, because the minimum gain must overcome the losses carried out of sustainable oscillation. Thus, the threshold gain specifies the minimum population inversion required to enable the lasing action.

The total losses of the system are due to a number of different issues, including transmission and scattering within the cavity, and absorption of the laser medium. The fraction of loss can be presented as: $^{-2}$, where L is the length of the laser cavity, and α is the single loss coefficient within the cavity. In contrast, the fraction of gain can be presented as: ^{2} .where g is the gain coefficient induced by the cavity over stimulated emission[22]. Hence, when the fractional loss is equal to the fractional gain, the threshold condition required to obtain a lasing status would appear as,

$$r_1 r_2 e^{-2\alpha L} = e^{2}$$

and

$$r_1 r_2 e^{2(-)} = 1$$

where r_1 and r_2 are the reflectivity on each side of the cavity. The threshold gain per unit length can be obtained by rearranging the above expression to give:

$$\alpha = +\frac{1}{2}\ln\left(\frac{1}{r_1 r_2}\right)$$

where $\frac{1}{2}\ln\left(\frac{1}{r_1 r_2}\right)$ represents the transmission loss through the cavity mirrors.Clearly, the above equation interprets the basic requirement to achieve the laser action, which is to raise the threshold gain until it overcomes the losses produced from the cavity.

In order to achieve population inversion, an external excitation needs to be performed. There are basically two ways of pumping electrons to conduction band, either exciting via optical injection, or electrical injection. In this case, electrical pump of laser devices has an advantage over optical injected method, as electrical excitation does not require additional light source with a stronger energy distribution. Thus, electrical injection laser is preferred and mainly carried out for industrial applications.

Here, the amount of injected current to achieve the laser threshold condition is called threshold current (I_{th}), which depends on the efficiency of electro-optical power conversion. As the laser structures vary from one to another, the threshold current can not exactly indicate the performance of a single laser device. Thus, the introduction of threshold current density ($J_{th}=I_{th}/A$), which is the threshold current per squarecentimetre, become an effective reference for determining the quality of a laser device. It indicates that by the same amount of current injection, the smaller the injection area is, the larger the current density. Therefore, nowadays the waveguides of laser devices are shrinking to a smaller and smaller size in order to achieve a more significant current confinement. Meanwhile, the laser geometries have also been modified to improve the current density. For instance, laser structures have be developed from the early-stage stripe lasers to ridge-waveguided lasers, and further to the rib-waveguided (deeply etched) lasers. By incorporating these developments in laser geometries, the threshold current density is significantly reduced.

1.5.3 Methods for Characterisations of Semiconductor Laser Diodes

Laser diode characterization can be broken down into five categories:

1. **Electrical** Measurement of light output, voltage drop, and photodiode monitor current. Derivative analysis of this data may also be performed.
2. **Spatial** Output light intensity profile in the far and near field and pointing angle of the radiation pattern.
3. **Spectral** Spectral data acquired to calculate spectral width and centre wavelength, and to observe mode structure.
4. **Optical** Measurement of astigmatism and other wavefront errors.
5. **Dynamic** Measurement of noise, inter-modulation distortion, rise time, fall time, chirping and device operation lifetime.

In our research, there are mainly two types of characterisations included, which are electrical and spectral characterisations.

For electrical characterisations, the most common of the diode laser characteristics is the L/I curve. It plots the drive current applied to the laser against the output light intensity. This curve is used to determine the laser's operating point (drive current at the rated optical power) and threshold current (current at which lasing begins). Typically, laser threshold will increase exponentially with temperature as $I_{th}\exp(T/T_0)$, where T is the laser temperature in degrees Kelvin and T_0 is the "characteristic temperature" of the laser. The efficiency of a diode laser is also derived from the L/I curve. It is most commonly expressed as slope efficiency and measured in units of mW/mA. The L/I characteristics may also be acquired in a low-duty-cycle pulsed mode. The increase in threshold and decrease in slope efficiency observed in the continuous wave data, as compared to the pulsed data, stems from the rise in junction temperature. This rise, due to the thermal resistance of the device, is typically 40 to 80°C/W. Typically, pulse widths used in this type of measurement are 100 to 500 nanoseconds, with a duty cycle of less than one percent. Unusually large differences between the continuous wave and pulsed L/I curves may suggest poor die attachment or a leaky junction, and are often an indicator of poor laser quality.

Apart from L/I characteristics, the I/V curve is also plotted to determine the electrical properties of the semiconductor materials and the metal contacts, including break-down

voltage, switch-on voltage, contact resistivity and series resistance. This characteristic is similar to the analogous characteristic of any other type of semiconductor diode and is largely invariant with temperature.

In case of spectral characteristics, it is normally focused on emission wavelength and spectral profiles. There are two basic types of spectral mode structures for diode lasers: singlemode and multimode. In the spectral context, these are longitudinal modes, which is highly dependent on the cavity lengths. Generally, 1300-nm and 1550-nm devices are multimode devices, with a spectral linewidth of about 3 nm FWHM.

1.6 Organisation of the Thesis

The organization of the thesis is as follows:Thedevelopment of the 1.3-μm quantum dot laser epitaxially grown on Si and Ge substrates is the main subject in this thesis. There are further developments of Si-based photodetectors studied here with similar epitaxial structures. Chapter 1 generally describes the scientific background and motivation of QD-based Si photonics. Principles of semiconductor physics and device characterisations are also introduced here.

Chapter 2 presents all the techniques used for epitaxial growth and device fabrication. An introduction of MBE system is firstly carried out, following by the description of reflection high-energy electron diffraction (RHEED), which is used for in-situ monitoring during the epitaxial growth. Thereafter, a few techniques required for the determination of material quality are explained, such as atomic force microscopy (AFM), transmission electron microscopy (TEM) and X-ray diffractometry(XRD). Subsequently, the challenges in epitaxial growth of III-V on group IV substrates are discussed. Lastly, the involved techniques of device process are listed.

Chapter 3 discusses the optimized growth conditions for InAs/GaAs QD lasers directly on Si substrate. The studies of the AFM, TEM and photoluminescence of the materials are involved in this chapter. Subsequently, the device fabricated out of this material is further tested and characterised with I/V measurements, room-temperature L/I, temperature dependent L/I and power dependent spectral analysis, just to name a few. In addition,

aslightly modified epitaxial structure on Si substrate is implemented as a Si-based photodetector with series of responsivity measurements.

Chapter 4 surveys the epitaxial growth techniques applied for the InAs/GaAs/Ge QD lasers, material studies and further device characterizations. The optimization of nucleation temperature is studied to understand effects of interface nucleation to the defects density. The device fabricated under the optimized condition is then bar-tested with both pulse and continuous-wave current injections, and further temperature dependently measured.

Chapter 5 deals with the theory and modelling of photonic waveguides for the design of ridge waveguide laser diodes. The guided wave theories are systematically described in this chapter. Furthermore, the ridge waveguides with different dimensions are simulated by FIMMWAVE mode simulator to optimize the mode operation within the ridge waveguide lasers.

Chapter 6 summarises the results presented in the previous chapters, highlights the most important aspects of the thesis. Further suggestions of future work are given in the final section of the chapter.

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Chapter 2

Techniques forEpitaxial Growth and Device Fabrication

This research project involves epitaxial material growth, device processing and characterisation. The quantum-dot samples were grown by using VeecoGen930 MBE facility at the Department of Electronic and Electrical Engineering, UCL. The III-V quantum-dot laser diodes on both Ge and Si substrates have been processed at London Centre for Nanotechnology and characterised at UCL. This chapter outlines the experimental work associated with the project.

2.1 MolecularBeamEpitaxy

Molecular beam epitaxy (MBE) is one of several methods of depositingsingle crystals. It was invented in the late 1960s at Bell Telephone Laboratories by J. R. Arthur and Alfred Y. Cho.MBE is an ultra-high vacuum epitaxial growth technique that operates by beaming atoms and molecules onto a substrate2.6.The most important aspect of MBE is the slow deposition rate (typically less than 1000 nm per hour), which allows the films to grow epitaxially. The slow deposition rates require proportionally better vacuum to achieve the same impurity levels as other deposition techniques.Firstly, solid sources in cells, known as Knudsen cells or effusion cells are heated to evaporate the growth materials. This forms

beams of homo-atomic molecules that are directed towards the substrate, which is heated and rotated for uniform deposition. The flux rates of the collision-free molecular beams depend on the temperature of the effusion cells. The flux rates are determined by an ion gauge and/or Reflection High-Energy Electron Diffraction (RHEED)[1]. The morphology of the growing surface is determined by the migration of the deposited species. The migration and hence morphology depends on the flux rates, substrate temperature, the surface material and its crystallographic orientation. The growth chamber of an MBE is kept at pressures in the region of 10^{-11}Torr in order to reduce the background pressure of contaminants. Mechanical shutters with fast actuation times can be used to deposit less than a monolayer of material. A schematic diagram of an MBE growth chamber is shown in Figure 2.1.

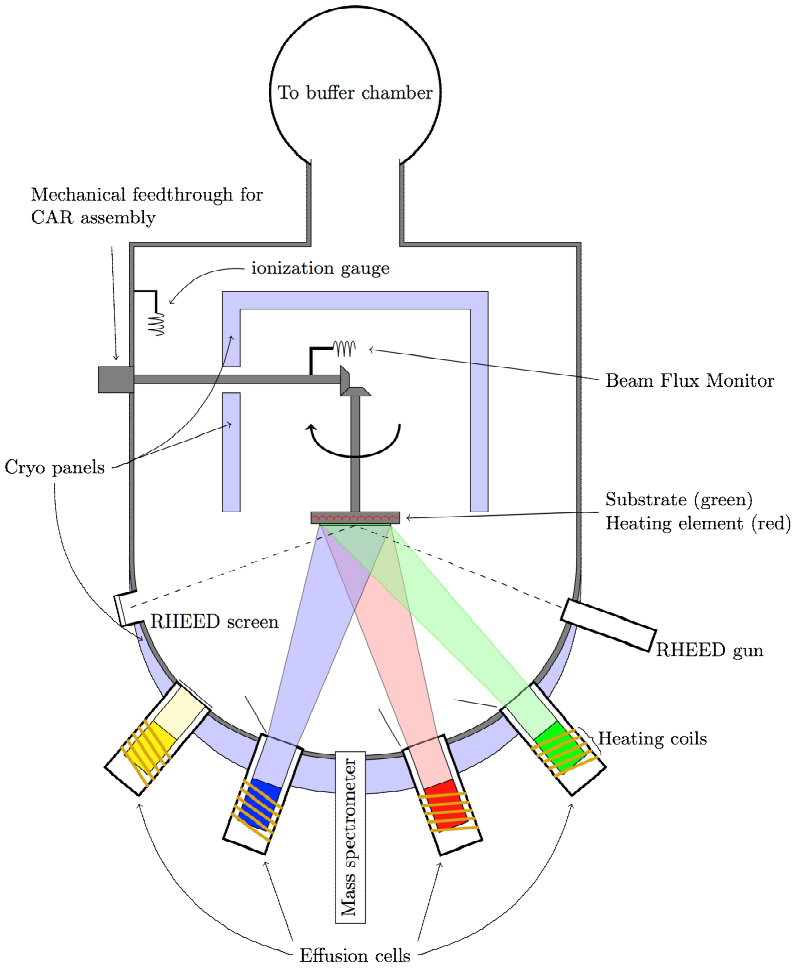


Figure 2.1 Schematic diagram of MBE growth chamber.

Although there are many existing epitaxial growth techniques as shown in Table2.1, MBE is the simplest way conceptually of fabricating semiconductor heterostructure process. Alternatively, another option to deposition by molecular beams is the hydrodynamic transport of material to the substrate from gas sources[1], such as metal-organic vapour phase epitaxy(MOVPE) and vapour phase epitaxy(VPE). There are also metal-organic molecular beam epitaxy (MOMBE), gas source molecular beam epitaxy (GSMBE) and chemical beam epitaxy (CBE) listed in Table 2.1.

The comparative advantages of MBE and MOVPE are the subject of frequent and often lively debate, due in part to their strengths and weaknesses being in many respects complementary. MBE is carried out at relatively slow growth rates in a controlled ultra high vacuum (UHV) environment for which in situ diagnostic techniques for the growing film are readily available, RHEED for instance.

Method	***Materials***	***Sources***	***Delivery***
MBE	III-V, IV	Elemental	Molecular
MOMBE	III-V	Metal-organic(III), Elemental(V)	Molecular
CBE	III-V	Metal-organic(III), Hydride, Organo-substituted Hydride(V)	Molecular
GSMBE	IV	Hydride, Chloride, Chloro-hydride	Molecular
MOVPE	III-V	Metal-organic(III), Hydride, Organo-substituted Hydride(V)	Hydrodynanmic
VPE	IV	Hydride, Chloride, Chloro-hydride	Hydrodynanmic

Table2.1: A glossary of epitaxial growth techniques

On the other hand, MOVPE relies on the hydrodynamic delivery of material to the substrate, so only optical techniques are appropriate for in situ diagnostics, which contain less information on surface morphology. Despite these differences, the choice between MBE and MOVPE is often dictated solely by material issues. For instance, the production of aluminium-containing heterostructures for optical applications(eg. AlGaAs lasers) is well suited to MBE but not to MOVPE, since the aluminium precursors used in MOVPE typically contain oxygen which, if incorporated into the material, act as a non-radiative recombination centre that degrades the performance of the laser. In contrast, for the production of materials containing phosphorus, MOVPE is usually preferred because the residual phosphorus from the solid source used for MBE condenses as white phosphorous,

which is highly pyrophoric. Although an MBE system can be modified with additionalphosphorous recovery to overcome this problem, MOVPE is still the most popular system for telecom laser fabrication mainly due to its low cost and fast production speed.

The use of gas source in VPE has several attractive features for the epitaxial growth of semiconductor heterostructures, such as room temperature operation, simple reactor and uniform molecular flux. MBE requires exactly the opposite conditions, with the need to cool the system with liquid nitrogen and a complex reactor. But the complex reactor also provides an operational advantage, because there is no depletion, the growth chamber does not need to be opened and exposed to air in order to replenish source material[1]. Lastly, there is a critical disadvantage over any VPE system that the gas sources can be extremely toxic. The major strength of MBE is that UHV environment enables the application of in situ surface analytical techniques to characterize the evolution of the growing material at various levels of resolution.

To summarize, MOVPE is heavily employed by industry due to ease of use, and scalability for fabrication. MBE ispreferable in research laboratories for producing complex and high-performance nanostructures.

2.2 Observation of Growth Kinetics and Surface Morphology

As mentioned above, an important operational advantage of the UHV environment of MBE is the wealth of analytic techniques available for examining the morphology of the growing surface in situ. The most prevalent of these utilize either diffraction or real-space imaging. In terms of diffraction techniques, there are reflection high-energy electron diffraction (RHEED), low-energy electron diffraction, helium-atom scattering and grazing-incidence X-ray diffraction [2]. In real-space imaging, most of techniques are based on electron microscopy, such as scanning electron microscopy (SEM),and transmission electron microscopy (TEM). There is only one exception called atomic force microscopy (AFM) based on detection of force induced by atom-atom interaction. With the combination of different types of microscopy, the methods of imaging strain fields, dislocations, the crystallographic orientation of the substrate and epi-layers, and the coherency and abruptness of heterogeneous interfaces can be provided extensively. In this section, three most common

methods used for characterisation of epitaxial growth will be introduced, which are RHEED, AFM and XRD, while only RHEED is the in-situ monitoring method can be applied.

2.2.1 RHEED

Surface electron diffraction is a standard method for examining the surface morphology with a much higher resolution than x-ray diffraction. Among all current existing surface electron diffraction methods, RHEED is the most suitable diagnostic tool for MBE. A RHEED measurement is carried out by shooting a high-energy (typically 10-20kV) beam of electrons at a small angle (0.5^{o}-3.0^{o}) [3]towards the surface of material. The reflected electrons interfere with each other and form a diffracted pattern on a phosphorescent screen.

There are mainly two advantages of using RHEED as surface analytic tool for MBE system:

1. Simple set-up, requiring only an electron gun and a phosphorescent screen.
2. The measurement is compatible with molecular beams emanating from the cells, and thus will not interrupt the growth process.

RHEED provides several types of information about the target surface, including crystallographic symmetry (from the symmetry of the diffraction pattern), the extent of long-range order (from the sharpness of pattern), and whether growth is precedingin a 2D or 3D mode. But the main application of RHEED is based on measuring the intensity of the specular beam for the growth rate. A periodic intensity oscillation can be recorded in this way due to the waveform of diffracted electrons being constructive and destructive interfered. In Figure 2.2(a), the uniformity and flatness of grown surface remains constant for the growth of each layer, resulting a stable specular intensity.Hence, a perfect sine wave oscillation can be observed. In contrast, an imperfect growth would lead to a decaying envelope of specular RHEED intensity as shown in Figure 2.2(b). Therefore, the layer-by-layer growth of MBE system can be monitored all the way through RHEED without any interruptions. By employing RHEED, the number of atomic layers deposited and phase of growth can be determined from the level of intensity. The peak of intensity oscillation implies a complete reflection from the surface indicating a flat and uniform surface.Once

material deposition starts, specular intensity drops as the reflected beam from the layer of depositing materials interferes with the beam reflected from substrate. The rougher the substrate is, the lower the specular intensity become. The specular intensity falls down to the lowest position, while half of the substrate is deposited with new materials.

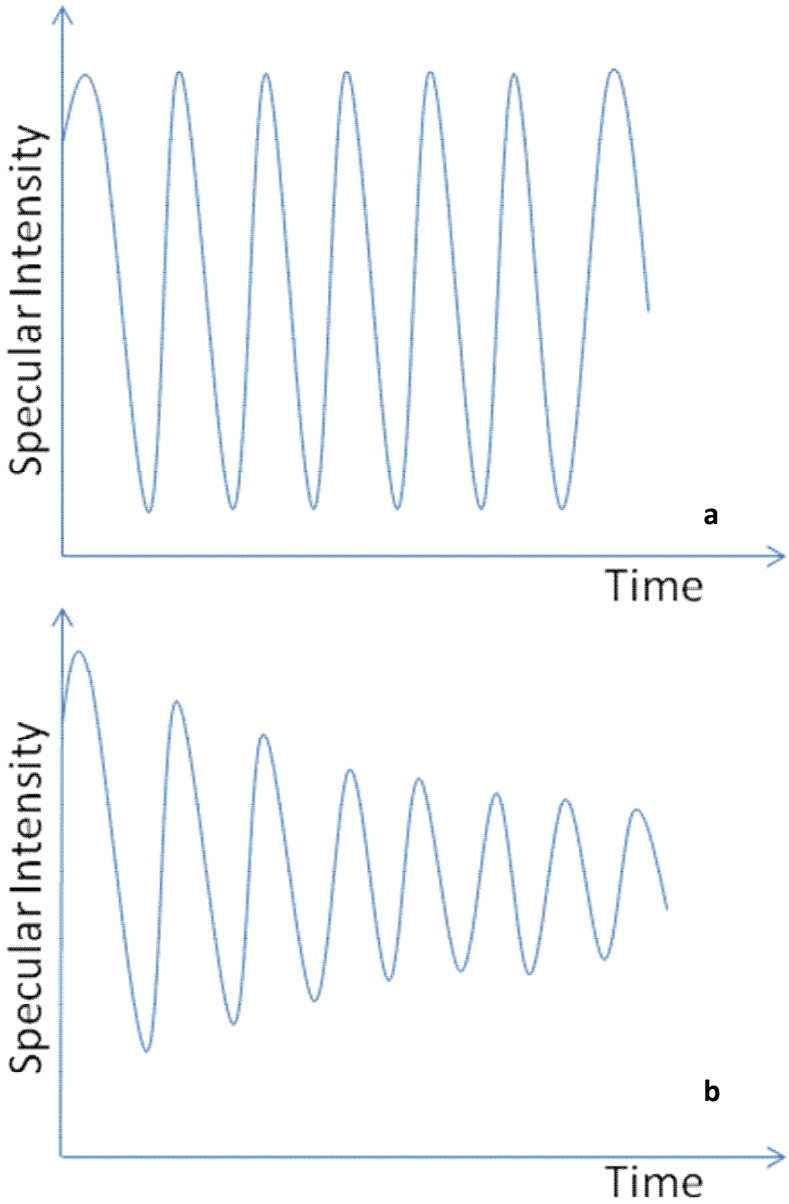


Figure 2.2: Illustration of specular RHEED oscillations from a) an uniformly growing surface and b) an imperfect grown surface.

Thus, the reflected beam from the substrate interferesdestructively with the reflected beam from the deposited layer. Once the second layer of material has covered the

substrate, the second peak intensity appears due to the constructive diffraction from the completely grown surface.

In the case of an imperfect growth, the roughness and flatness of the surface may vary for each layer of growth. Therefore, the peak intensity of each specular oscillation would decay as time passed to form a decayed envelope. Hence, the quality of the growth of quantum heterostructure can be fully characterizedwithin the process, including surface roughness, flatness, uniformity, density and thickness.

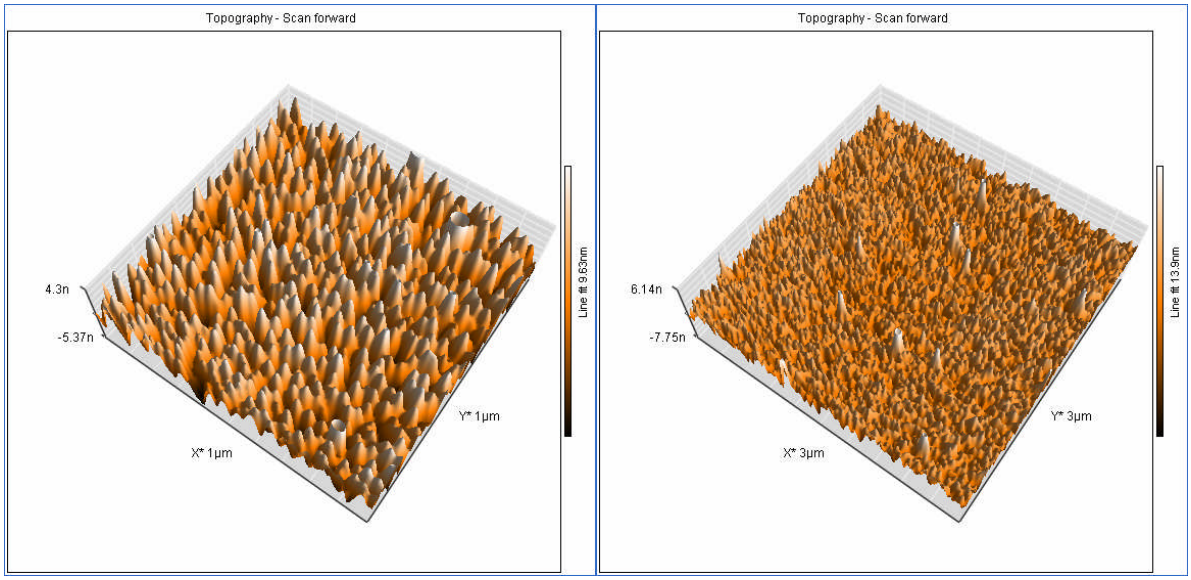
2.2.2 AFM

Before introducing AFM, a similar technique will be discussed here first. The scanning tunnelling microscope (STM), invented in 1982 by Gerd Binning and Heinrich Rohrer at the IBM Research Laboratories in Switzerland [3], uses an atomically sharp tip placed sufficiently close to a surface to produce an electron tunnelling current between the tip and the surface. By measuring this current as the tip scans the surface, images of the surface are obtained which, under favourable circumstances, has a lateral resolution of 1Å and a vertical resolution of 0.1Å.

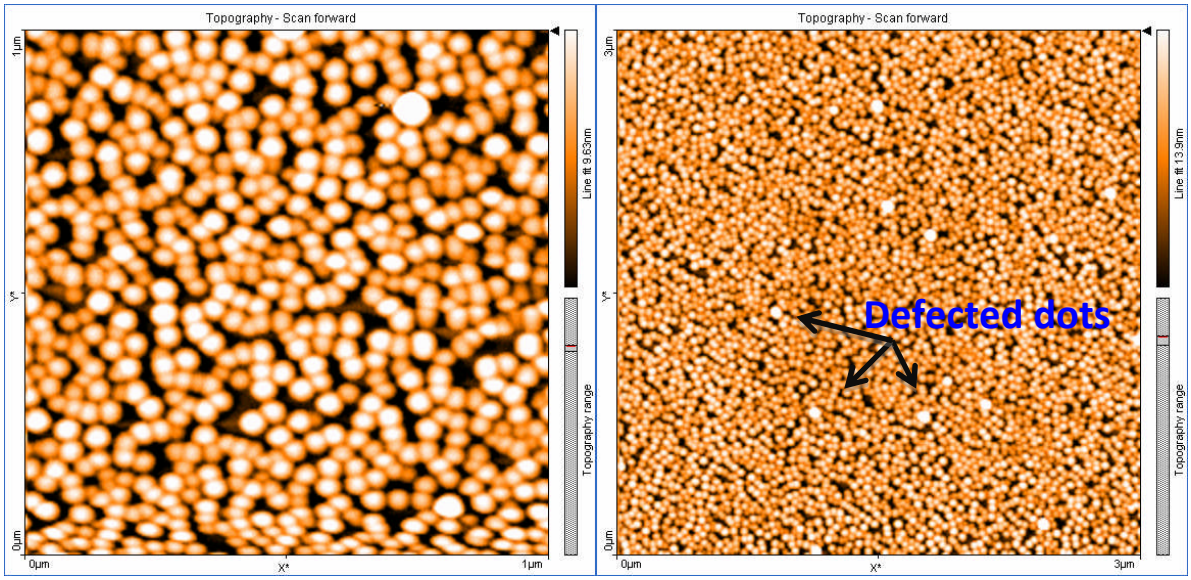
The STM revolutionizes the field of surface science and has seen applications that extend far beyond the traditional boundaries of condensed matter physics. Its impact on fundamental studies of epitaxial growth has also been immediate and far-reaching. In the case of this project, the creation of quantum dots produces broken, dangling bonds and misfit dislocations, which leave the surface in an unstable high-energy state. While the tip scans over the surface, an electron tunnelling current occurs with the current transfer from the surface energy to the tip. Hence, the surface information and image can be obtained by analyse the amplitude of the tunnelling current.

When the tip of an STM is brought close to a surface, the atoms near apex of the tip exert a force on that surface which is of the same order of magnitude as the interatomic forces within the surface. This phenomenon is the origin of AFM. An STM tip, mounted on a flexible beam, is brought just above a surface. The force between the surface and the tip causes a small deflection of the beam. The surface is then scanned while a constant force is maintained between the tip and the surface with a feedback loop similar to that used in the

operation of an STM. Because the STM relies on the analysis of the tunnelling current, it is sensitive to the density of electronic states near the Fermi level of the sample. Thus, the density of states must be non-zero, indicating that the sample has to be a conductor. With this restriction, the available choices of materials are limited for STM.



a) b)



c) d)

Figure 2.3: AFM images of InAs quantum dots grown on InGaAs wetting layer, a) and b) are the 3D image of InAs QDs within 1µm^2 and 9µm^2 area, c) and d) are the 2D images of InAs QDs within 1µm^2 and 9µm^2 area.

Additionally, since the tunnelling current decreases exponentially with the tip-sample distance, an STM tip must be placed within few angstroms to the surface in order to maximize the resolution of the image.Employing a similar tip, AFM responds to interatomic force rather than tunnelling current. This interatomic force is called Coulomb interaction, which is a cumulative effect of all electrons[3]. AFM operates at much larger distances from the surface, typically 50-150 angstroms. Hence, a wide range of selection of material can be measured, including fragile and non-conducting samples in comparison with STM. Finally, AFM does not require an UHV environment, normally operating in ambient atmosphere or in a liquid. Here, Figure 2.3 shows the AFM images of high-density InAs quantum dots grown on GaAs substrate. The bean shape spots in the pictures are InAs quantum dots grown by the solid source Veeco GEN930 MBE at UCL. In Figure2.3, the area density of quantum dots is about 4.3×10^{10} cm^{-2} per layer measured by AFM on an uncapped QD layer. InAs quantum dots have a height between 6 and 10 nm and typically are about 30nm wide as shown in the images above, and the bright white spots observed are the defected dots generated due to the strain formed between dots and the wetting layer. The lower the defects density is, the better the optical performance is.

2.2.3 X-ray Diffractometry

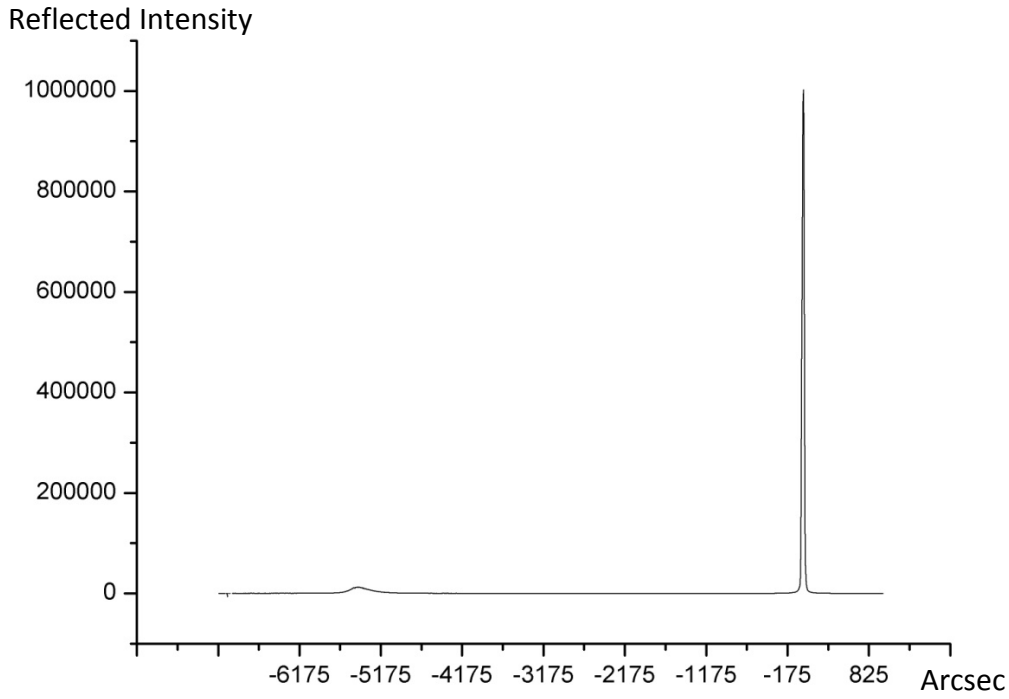
X-ray diffractometry (XRD) is one of the most essential techniques to determine the parameters of epitaxial layers. The information that can be obtained from the X-ray diffractomety includes the composition of ternaries, mismatch of quaternaries, mis-orientation, layer thickness, tilt, relaxation, indications of strain, curvature and stress, and area homogeneity. By characterising the epitaxial structures with XRD, epilayers can be determined to be mismatched, defective, non-uniform and bent[2]. All these distortions of crystal structures would be correlated with degradation of device performance. Especially for III-V semiconductors, the epilayers are nowhere near as perfect as silicon, either in defect concentration or in composition uniformity. The X-ray rocking curve carries all the required information for determining the quality of epitaxial structures. Table 2.2 shows the effect of substrate and epilayer parameters upon the rocking curve.

Material Parameter	**Effect on Rocking Curve**	**Distinguishing Features**
Mismatch	Splitting of layer and substrate peak	Invariant with sample rotation
Misorientation	Splitting of layer and substrate peak	Changes sign with sample rotation
Dislocation content	Broadens peak	Broadening invariant with beam size No shift of peak with beam position on the sample
Mosaic spread	Broadens peak	Broadening may increase with beam size, up to mosaic cell size No shift of peak with beam position on the sample
Curvature	Broadens peak	Broadening may increase with beam size Peak shifts systematically with beam position on the sample
Relaxation	Changes splitting	Different effect on symmetrical and asymmetrical reflections
Thickness	Affects intensity of peak Introduces interference fringes	Integrated intensity increases with layer thickness, up to a limit Fringe period controlled by thickness
Inhomogeneity	Effects vary with position on sample	Individual characteristics may be mapped

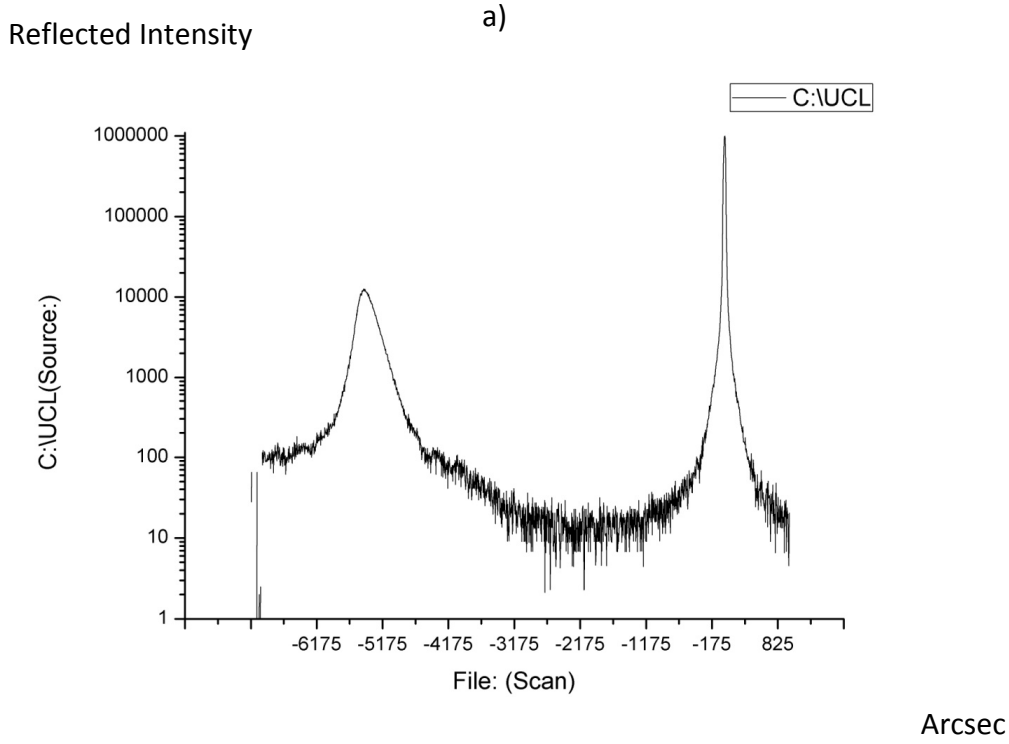
Table2.2: The effect of substrate and epilayer parameters upon the rocking curve.

Among these common defects shown in Table 2.2[2], Mismatch is the most vital parameter to determine, both in itself as a measure of strain in the epilayer but also because it allows us to determine composition for ternary compounds and hence infer the bandgap. Layer thickness is also an important characterisation parameter for device

behaviour. Therefore, the subsequent growth can be further optimised by those parameters obtained from XRD measurement.



a)



b)

Figure 2.4: XRD result of GaAs direct epitaxy on Si in a) linear scale and b) log scale.

In the case of the epitaxial growth of GaAs on silicon substrate, a splitting between GaAs and Si substrate peaks can be observed as shown in Figure 2.4. Due to the lattice mismatch between GaAs and Si, GaAs epitaxial layers are heavily strained. Therefore, the broaden peak of GaAs layers would occur in this case. The linewidth of bulk GaAs XRD peak is normally around 10 arcsecs, and 8 arcsecs for silicon correspondently. In contrast, a defective, strained or stressed crystal can result a much broader XRD peak due to unexpected scattering and interference from defects and dislocations. Consequently, a narrow linewidth indicates a high quality epitaxial layer (fewer defects). It is clear that In Figure 2.4 the substrate peak, which is perfect silicon crystal, is extremely narrow with a linewidth around 8 arcsecs. The narrowest XRD linewidth of a 2µm thick GaAs epitaxial layer grown on silicon substrate that has been claimed is 200 arcsecs[4]. In our recently established advanced growth techniques, we have been able to achieve 162 arcsecs by direct epitaxial growth of GaAs on Silicon, which present epitaxial layers with low defect densities. XRD is also a useful tool for epitaxial growth of strain-balanced heterostructures, such as superlattices andInAs/InGaAsdots in wells (DWELLs).

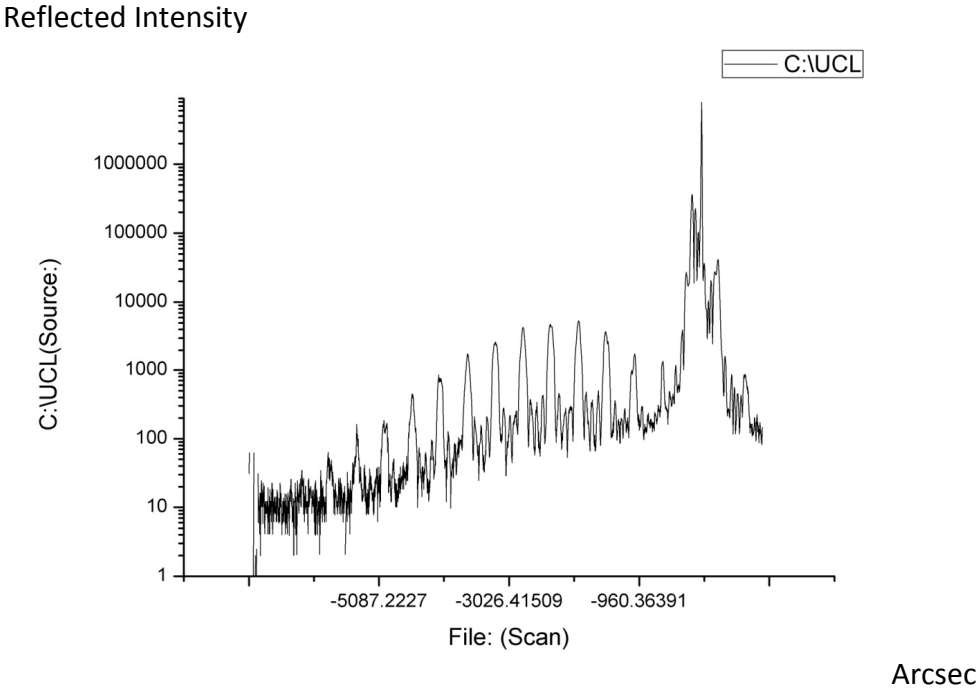


Figure 2.5: XRD result of an InAs quantum dot laser structure on GaAs substrate

Figure 2.5 is the XRD rocking curve of an InAs quantum dot laser structure, which contains many fringes generating from the GaAs/InGaAs multiple quantum wells, where the

sharpest peak is the GaAs, and AlGaAs cladding layer is the one next to it.As InAs quantum dots layers are relatively thin, the rocking wave of quantum dots will not be observed. But a broader fringe of a quantum well will appear correspondingly due to the strain formed between dots and wetting layer, and GaAs.

2.3 The Growth and Optical Characterization of Quantum Dots

The fabrication of heterostructures requires growing crystalline materials on the surface of different materials, a process which is known as heteroepitaxy. But a useful starting point for appreciating the complexity of heteroepitaxial phenomena is a conceptual framework for homoepitaxy, that is the growth of material on a substrate of the same material. Differing from homoepitaxy, there are heteroepitaxial effects to be considered, such as segregation, alloying and the relaxation of misfit strain[6].

Generally in the case ofgrowing quantum wells it is arranged that the well, barrier and substrate materials have the same lattice constant. For instance, GaAs quantum wells with AlGaAs barrier can be grown on GaAs substrate. However to strain a material requires energy. If we try to grow a semiconductor, that has a very different lattice constant to that of the substrate, the grown film will be strained. Hence, as the thickness of the film increases, energy will build up. Eventually there is sufficient energy to break the atomic bonds of the semiconductor and dislocations form. Beyond this point the semiconductor can grow with its own lattice constant, and strain energy no longer builds up.The thickness of semiconductor that can be grown before dislocations form is known as the critical thickness. The critical thickness is a function of the semiconductor being grown and also the degree of lattice mismatch between this semiconductor material and underlying substrate. Dislocations provide a very efficient mechanism for non-radiative carrier recombination, thus it is important not to exceed the critical thickness.

Quantum dots grown by MBE are currently based inherently on the method called Stranski-Krastanov growth[5], also known as layer-plus-island growth. The growth of quantum dots is mainly a transition from layer-layer growth to layer-island growth, influenced by lattice parameters and surface energies of the substrate and grown film.For instance, the most common quantum dots used for telecom lasers are the Stranski-

Krastanov growth [3](2D to 3D transform) of InAs on GaAs with 7% misfit. When InAs is first deposited on GaAs it grows as a highly strained, flat layer (2D growth). However for certain growth conditions before dislocations start to form, the growth changes to three dimensions in form of small islands. These islands form the quantum dots and sit on the original two-dimensional layer, known as the wetting layer. This process of quantum dots formation is caused by a trade-off between elastic and surface energy. All surfaces have an associated energy because of their incomplete atomic bonds. The surface energy is directly proportional to the area of the surface.Hence the surface after islands start to form has a greater energy than the original flat surface. However within the islands the lattice constant of the semiconductor can start to shift back to its bulk value (Figure 2.6), hence reduces the elastic energy. The increment in surface energy thus relaxes the misfit induced elastic stretching, which leads to the transformation to three-dimensional growth representing the most favourable energy state. These are the main mechanismsfor producing self-assembled quantum dots.

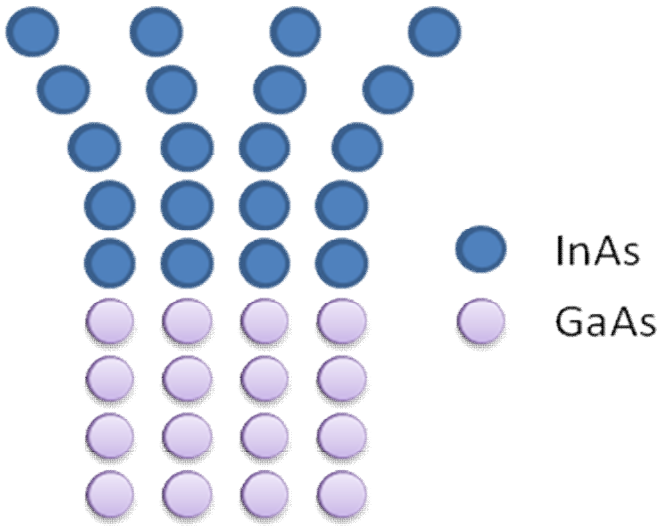


Figure 2.6: Change in the lattice spacing for atoms in a self-assembled quantum dots heterostructure due to lattice mismatch as thickness increases.

2.4 Challengesof GaAsDirect Epitaxial Growth on Silicon

The most severe problems in III–V on Si integration are the formation of high-density threading dislocations (TDs) and anti-phase domains (APDs)[7]due to the lattice mismatch and polar/non-polar interface between III–V compounds and Si substrate.

The generation of APDs from the interface remains to be the problem that causes the degradation in quality and roughness of epitaxial materials. The formation of APDs is caused by polar crystals grown on non-polar crystals. Since APDs are compromised of planes of wrong nearest-neighbor bonds, they are electrically active defects known to cause carrier scattering and non-radiative recombination[8]. As a result, any effort to grow practical GaAs/Si and GaAs/Gedevices must address the possibility of antiphase disorder and the approaches to suppress it.Instead of having continuously propagating APDs, the substrate with 4^{o} offcut towards [110] plane has helped to ensure that the APDs are confined only close to the III-V/IV interfaces as shown in Figure 2.7, where the red dashed lines cutting the Ga-Gabonds represent the APDs.

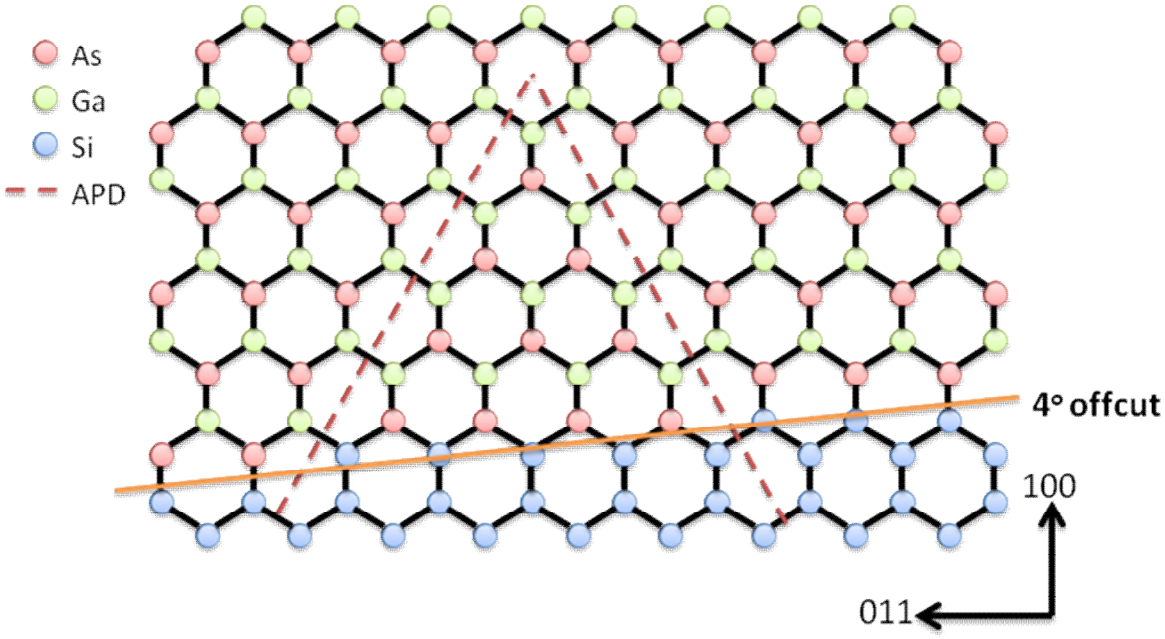


Figure 2.7: A diagram showing the formation of APDs.

As an offcut angle is increased, the density of steps and width of surface terraces decreases, a factor that may by itself promote early self-annihilation of APDs. As shown in Figure 2.7,offcut substrate favorsa single domain reconstruction, which extends to single-domain GaAs nucleation.

It has been proved that the primary challenge of III-V/Si integration is the formation of high-density TDs due to the lattice mismatch between III-V compounds and Si. The lattice mismatch between GaAs (InP) and Si is 4.1% (7.5%). Typically, the TD density resulting from

direct growth of GaAs or InP on Si is of the order of $10^{10}/cm^2$, which is much higher than the residual TD density ($\sim 10^3/cm^2$) found in bulk GaAs and InP wafers. Usually, TDs are present on the surfaces of the interfacial layers and propagate though the eptiaxially grown structures above to the active layers.Therefore, TDs are well known to act as nonradiative recombination centres and to promote dark line defects in the operation of semiconductor laser diodes, hence reducing optoelectronic conversion efficiency and device lifetime. Because the presence of TDs can seriously degrade device performance, minimizing the density of TDs has been the main challenge for III-V epitaxial growth on Si and Ge substrates. To improve the performance III-V quantum-well (QW) lasers on Si substrate, several different approaches have been extensively investigated in the last two decades. During this project, we found that the QW dislocation filter layers and the initial III-V nucleation temperature play an important role to suppress the formation of TDs. To investigate the effectiveness of techniques we used for minimizing the density of TDs, etch-pit density (EPD) and cross-sectional transmission electron microscopy (XTEM) are the main metrology in the project for monitoring the TD density variation, which will be discussed in detail in Chapter 3.

2.5 Device Fabrication

The fabrication of lasers requires several stages including photolithography, wet chemical etch, electrode metallisation, annealing and cleaving to produce the final device. In this section, the different stages of fabrication will be discussed and further explained the preference in each case.

2.5.1 Procedures of Device Processing

The stages required to fabricate the device are:

- ✓ Cleaving – The creation of weak points along the samples primary crystal facets to obtain desired size for processing.
- ✓ Wafer preparation – To purge the wafer of organic contaminants, the wafer is typically immersed in acetone and iso-propanol, then followed by ultra-sonic bath and hot plate

baking for dehydration. A further oxygen plasma process can be taken as an option to improve photo resist adhesion.

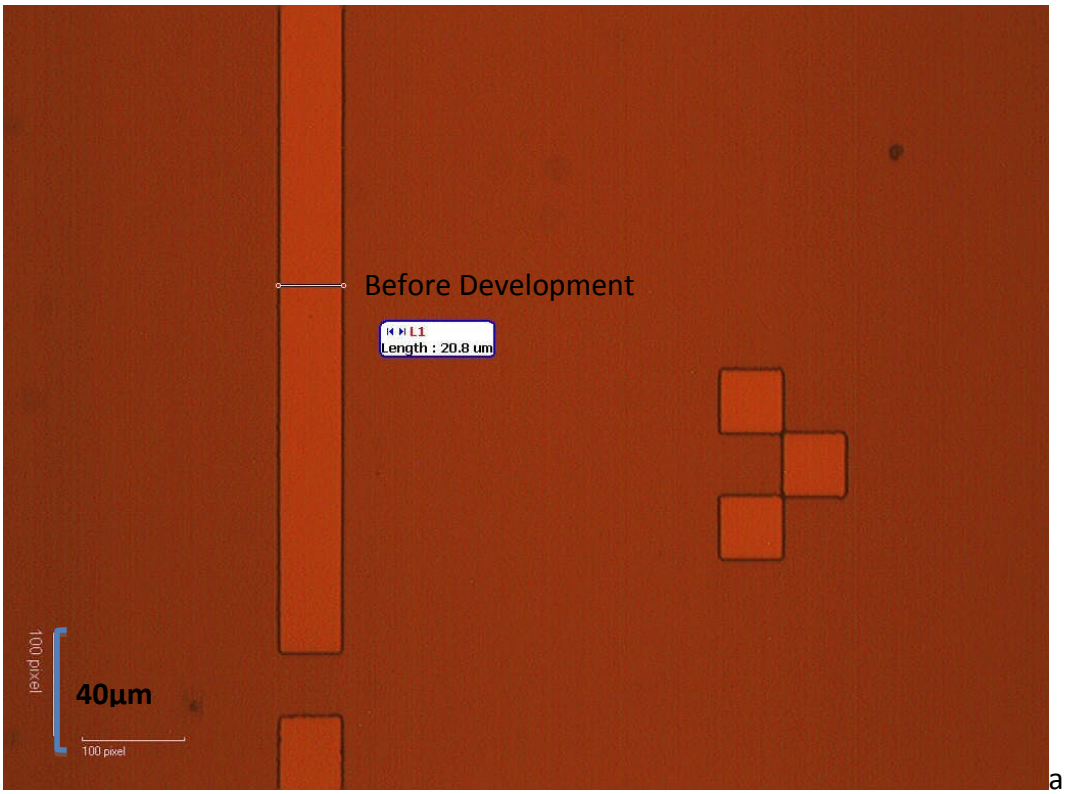
- ✓ Photolithography – To define the photo resist pattern for
  - ◆ Wet chemical etching of semiconductor material for mesa structure
  - ◆ Deposition of dielectric material(SiO2 or SiN) for passivation
  - ◆ Lift-off for metal deposition
- ✓ Wet chemical etching – Remove unwanted semiconductors from a pattern sample to produce mesa structures or open the depositing window of electrodes
- ✓ Metallisation
  - ◆ QD laser on GaAs – The deposition of N (Ni/GeAu/Ni/Au) and P contact metals (Ti/Au)
  - ◆ QD laser on Ge – The deposition of N (Ni/GeAu/Ni/Au) and P contact metals (Al)
  - ◆ QD laser on Si – The deposition of N (Cr/Au) and P contact metals (Ti/Au)
- ✓ Thinning – Reduce the thickness of substrate to an optimum level (typically 100um) for convenience of cleaving process and lower substrate resistance.
- ✓ Annealing – Fixed temperature heating to allow metal diffusion, and thus produce metallic alloy, such as Cr/Au or Ti/Au. A good metal-semiconductor interface can be subsequently produced to reduce ohmic contact resistance.
- ✓ Scribing – Create high quality facet along crystalline axis for cavity formations.

2.5.2 Photolithography

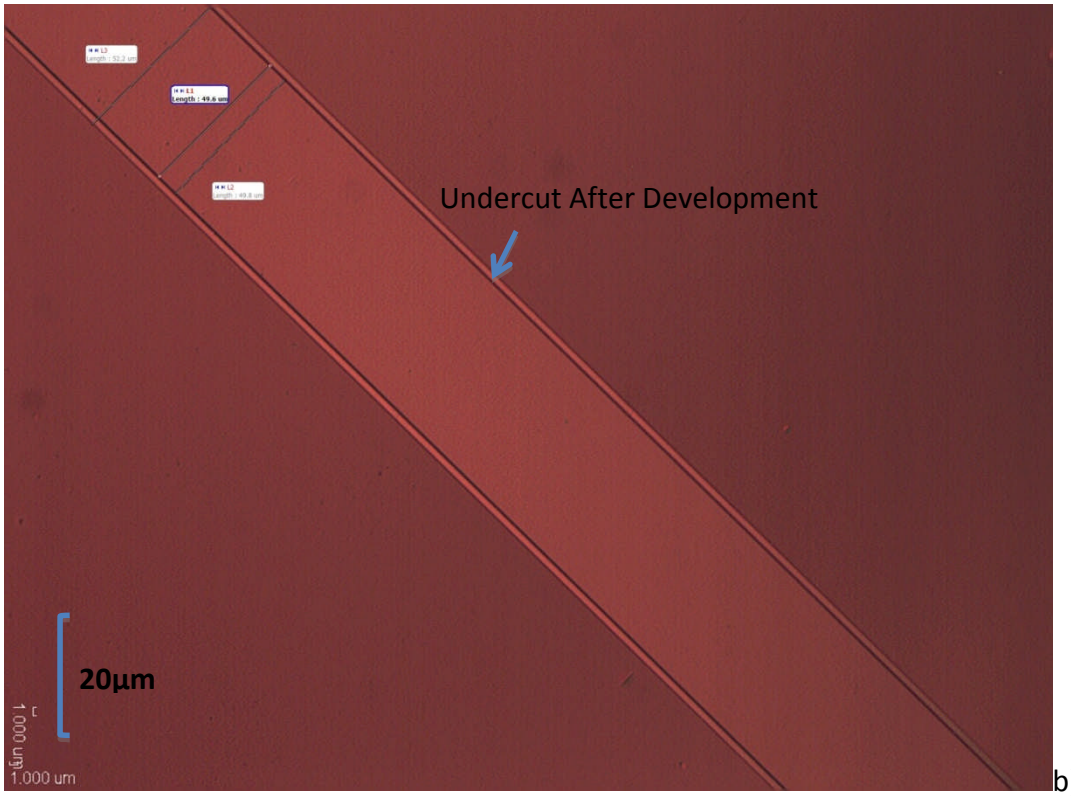
Photoresist is a light sensitive material, which can be deposited onto the sample with a spinner. By applying an UV light exposure with a patterned mask, following a chemical development, photoresist is prepared with patterns to prevent metal deposition or chemical etching in required regions. In general, the process involves the following steps:

- ✓ Resist deposition – Spin a small amount of photoresist solvent on the sample at a set speed;
- ✓ Prebaking – The photoresist is then baked to form a more stable chemical structure;
- ✓ Mask Aligning – The mask with desired pattern is aligned on the sample by using microscope, and then is brought in close contact to the sample. The pattern is transfer to the resist by a fixed time UV exposure;

✓ Image Development – The unwanted area on the sample is removed by dipping in the developer(an alkaline based solution).



a)



b)

Figure 2.8: a) 20um wide stripes for contact window definition,b)Photolithography for lift-off has created a significant undercut(where the double line indicates the undercuts).

The selections of UV exposure time, resist thickness and developing time are all based on the feature size of patterned structure. In my case, the optimised recipe is listed in part 2.5.1. Images in Figure 2.8 are the resist patterns for contact window definition and lift-off, where image in Figure 2.8 is a 20um wide stripe left open on the laser material. The contact metal can be further deposited in this open area. Normally, in the case of broad area laser, there is a thin layer of SiO_2 deposited on the sample for passivation. After this lithography, the metal contact window is open, but an oxide etch is required to remove the SiO_2 left on the p-type wafer surface. Thus, metal can be placed in a direct contact with semiconductor for current injection.

In order to have metals only deposited in the contact window, an extra lithography to create undercuts for lift-off is necessary. Undercut is one of the techniques used during lithography to create a platform for removing metals on the unwanted materials after metal deposition. Otherwise, the contact will cover the whole sample surface with resist remaining underneath, which cannot be removed and stick on the sample permanently. Image in Figure 2.8b has shown the undercuts produced after special lithography technique. This undercut structure will allow acetone to reach the photoresist during lift-off process. Therefore, metal deposited on top of the resist will be completely removed, leaving only the part of metal with direct contact to the sample (the area of contact window).

The process with cross-sectional images is shown in Figure 2.9, where the left picture is the undercut created by LOR double layer lithography. The middle one shows the metal deposition on sample and resist before the lift-off. The last image is the final contact metal left in the desirable position on the sample by removing the resist through acetone immersion(lift-off process).

Figure 2.9: The process of creating undercut and lift-off

2.5.3 Wet Etching

For semiconductor devices, such as a semiconductor laser, a wet etch is an essential technique to create a mesa for current and optical confinement. Photolithography has produced a mesa pattern to protect the area that is not required to be etched. In the case of laser fabrications, there are mainly two steps that require wet etching. One is SiO_2 etch(HF) for contact window definition, and the other is mesa etchfor creating waveguides.

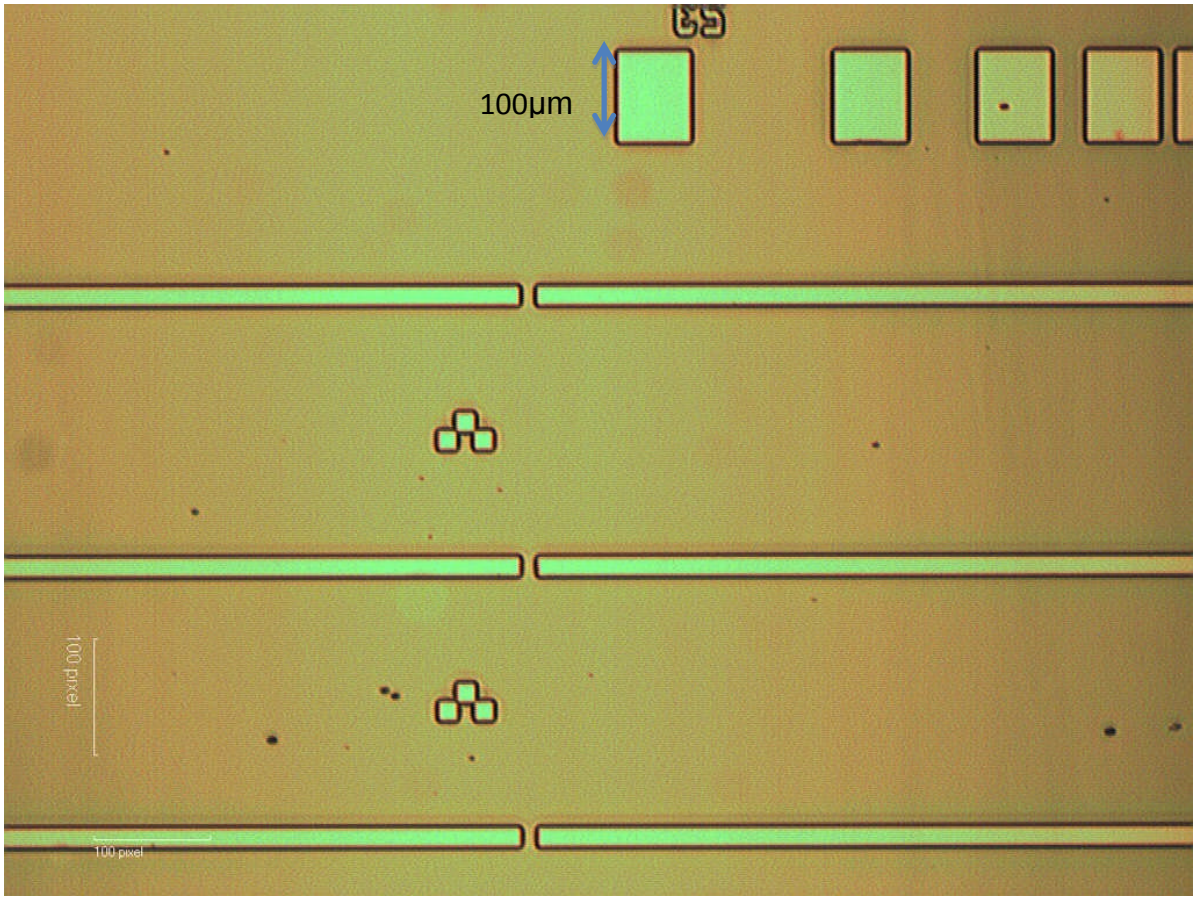
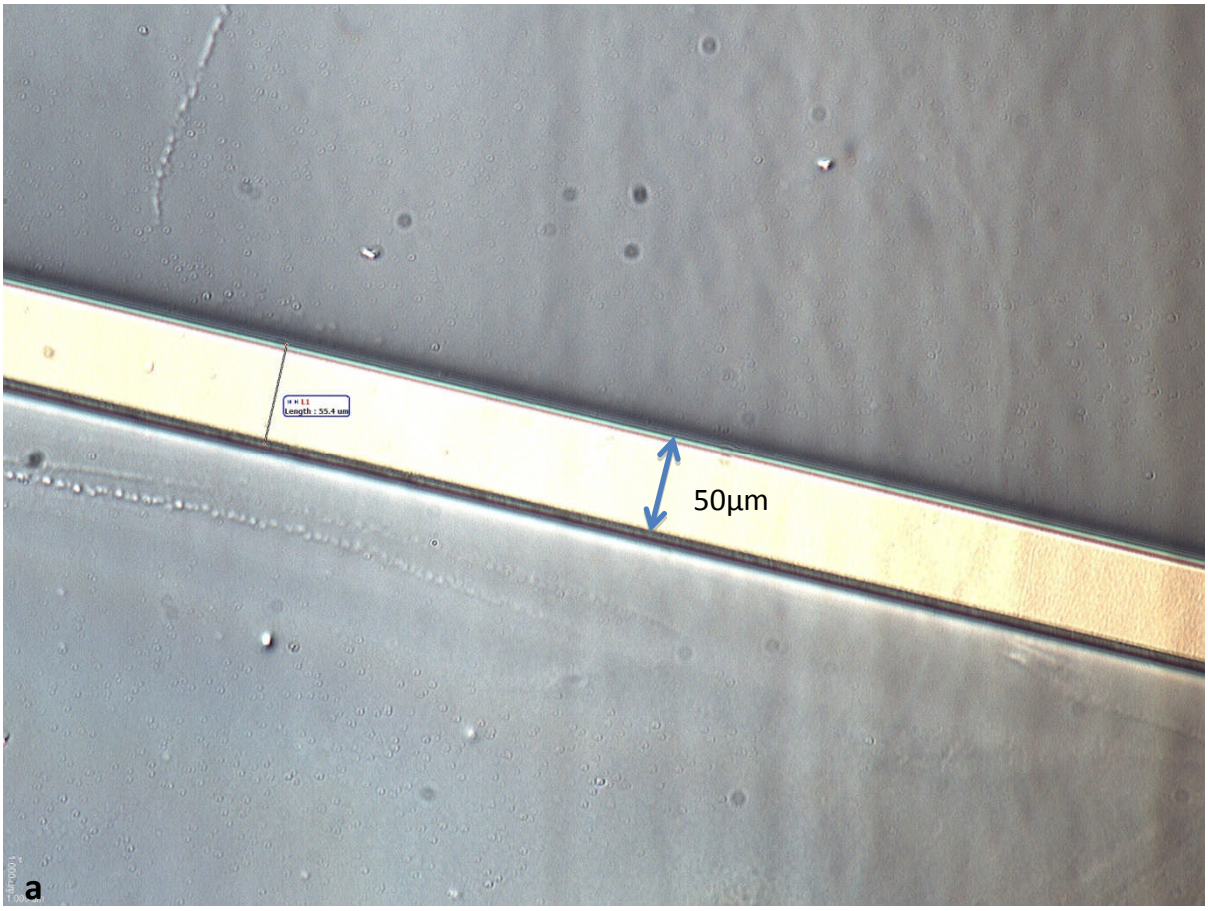
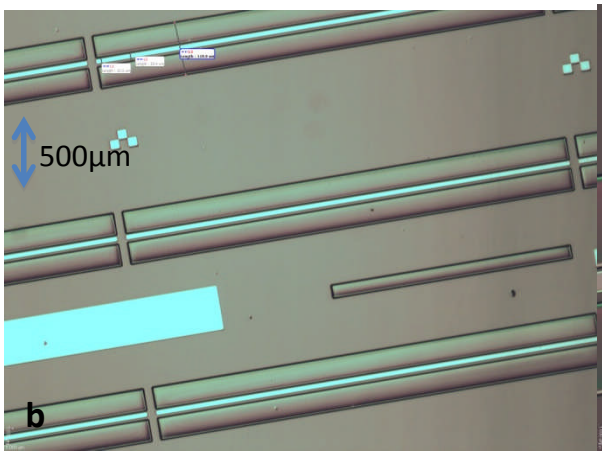


Figure 2.10: A sample for making stripe lasers with 200nm SiO_2 deposited on top. The bright stripes in the picture are contact windows with SiO_2 etched.

The key point of wet etching is to obtain a good control of the etch speed by using the etchant with a properly selected concentration. An inappropriate selection of etchant can also result a rough sidewall during etching. In the case of oxide etch, Buffered Oxide Etchant (BOE) is applied to remove the passivated SiO_2 in the contact window area (Figure 2.10). BOE is the mix of HF (Hydrofluoric Acids) and NH_4F (Ammonium Fluoride) in the ratio of 1:6, which is normally used for oxide removing of SiO_x and GeO_x. Differing from oxide wet etch,

III-V semiconductor selective etch is extremely sensitive to the etchant concentration and combination. A ridge waveguide production does not require selective etch. A III-V universal etchant or called Adachi etchant (Analar Potassium Dichromate: Analar Acetic Acids: AnalarHydrobromic Acid = 1:1:1) can be thus used to etch all the way down to the active region with one etchant only.





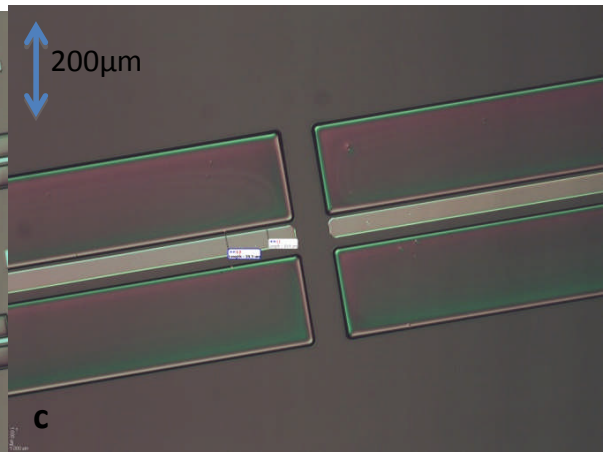


Figure 2.11: III-V semiconductor etching for creating ridge waveguide a)50um wide ridge with shallow etch in the depth of 0.8 um, b)20um wide rib waveguide with 1.8um deep etch down to the active region, c)Closer view of image.

Alternatively, a relatively weaker GaAs/InGaAs etchant (H_3PO_4:H_2O_2:H_2O = 1:1:3) has also been used to achieve better control of the etching depth and sidewall roughness.The contacting metal will be further deposited in this area to make an Ohmic contact to p-doped GaAs.

The etchant used here is oxide buffer etchant as mentioned above with an etch rate of 3.5nm/sec.A 60 seconds etch should remove all SiO_2 in the contact window, but normally an extra 10-20 seconds is added in order to achieve over-etched contact window with no oxide left on the surface of GaAs.

Figure 2.11 is the ridge waveguide produced by III-V semiconductor etching using Adachi etchant. A 50μm wide ridge with 0.8um etching depth is shown in Figure 2.11a, and an optional narrower 20um ridge with 1.8um etching depth is also processed as displayed in Figure2.11b and c. The etch rate of III-V semiconductors is difficult to control as the composition of InGaAs and AlGaAs varies in the different layers of laser structures. The quality of grown materials is also an important factor effecting the etch speed down the structure. Therefore, a test sample with same quality and structure is always required to determine the etch conditions.

2.5.4 Metallisation

The deposition of metal on III-V semiconductor materials can be achieved either by thermal evaporation or E-beam evaporation. For conventional GaAs based QD lasers, Ti-Au is deposited as a p-contact metal by using E-beam evaporator, and Cr-Au is selected as a n-contact metal by thermal evaporation method. During this process, the selection of metal contact and lift-off techniques appears to be extremely important. Cr-Au has been proved to be a good Ohmic contact metal for n-type substrate. Au-Zn-Au is also a good candidate for make p-type metal contact, but gold has a very poor adhesion to III-V semiconductors. Thus, an alternative choice would be Ti-Au, which can also provide a high-quality p-type contact, but requires E-beam evaporation.

Once the contact metals are selected, a proper metal lift-off is required to deposit metal contact at specific positions. The process of creating undercuts and further metal lift-off is described in section 2.5.2. There are a few different techniques to achieve this. One is Chlorobenzene soaking, which hardens the surface of photoresist by baking Chlorobenzene soaked resist. Once the sample is developed, the surface is attacked less by the developer, and the photoresist underneath develops faster as that region has no direct contact to Chlorine Benzene. But Chlorine Benzene is an extremely toxic solvent, thus, an alternative LOR double layer lift-off technique is developed correspondingly.

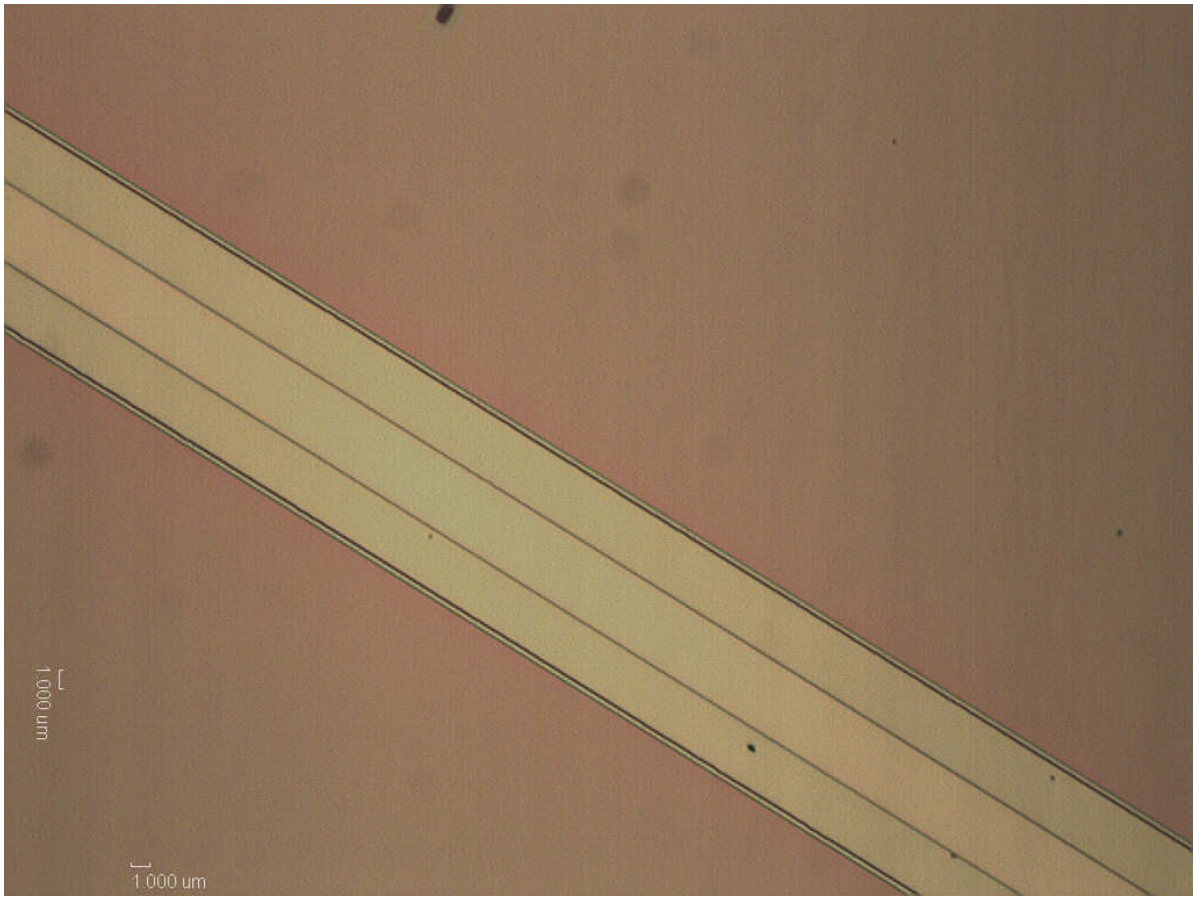


Figure 2.12: Undercuts produced for metal lift-off on a 60um wide contact pad.

By applying this LOR double layer lift-off technique, the lower layer of LOR has a faster developing speed, and the top layer of normal Shipley 1805 (a positive photoresist) develops at a relative lower speed. An undercut can be easily produced by controlling the developing speed of LOR layer, which depends on the baking temperature (typically from 150-200^{o}C).

In Figure 2.12, we can easily observe an extra 1um extension at each side of the contact stripe, where the undercuts are, because resists are transparent. A 20um wide stripe in the centre is position of contact window, where the metal will be contacted with. The wider stripe in the picture is the 60um contact pad for contact metal to settle, but only the 20um wide contact window in the centre will be conducting to the p-type GaAs. With a successful lift-off after metal deposition, a 60um wide metal contact pad will be left in alignment with the contact window as shown in Figure 2.13. Thus, current can be injected through this p-contact metal.

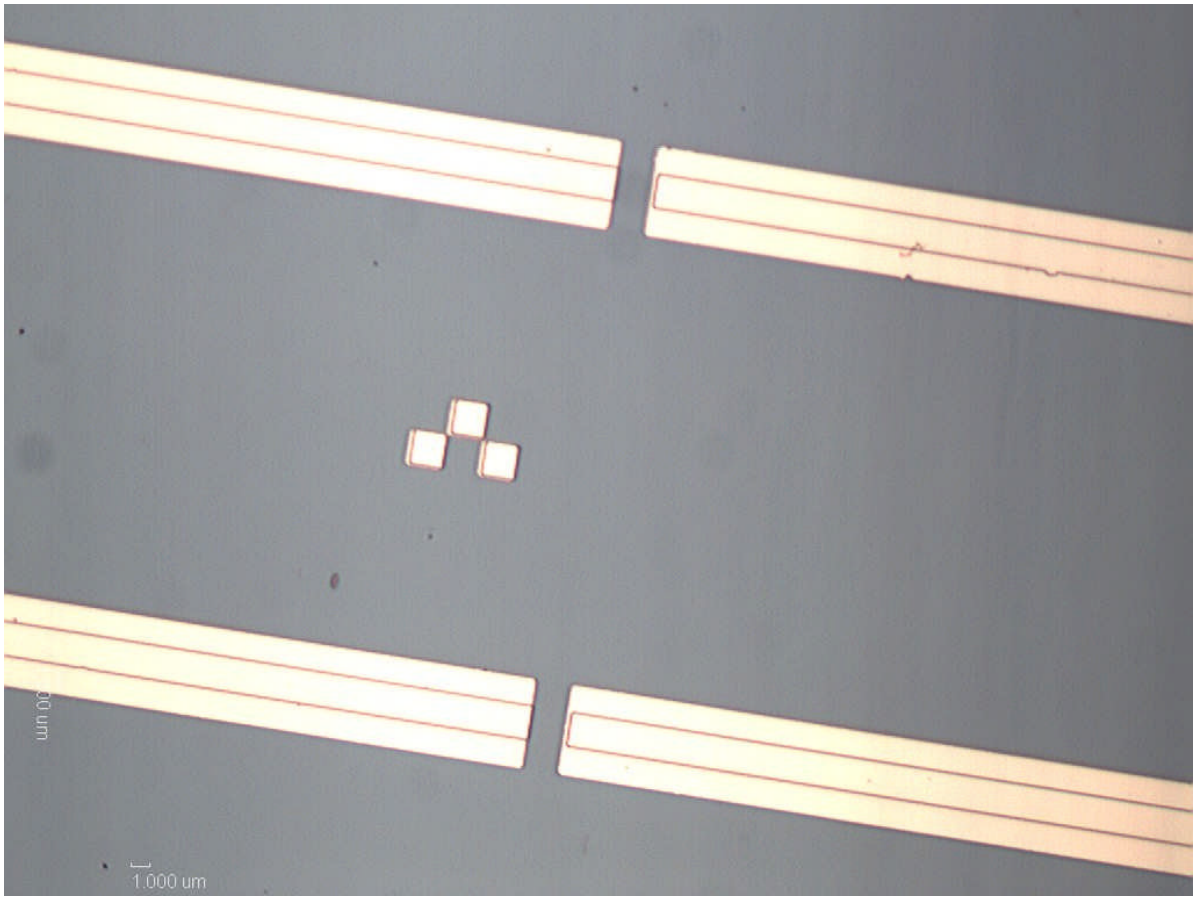


Figure 2.13: Successful metal lift-off.

2.5.5 Annealing

In theory, Ti/Au metal contacts should make a good Ohmic contact on the p-type GaAs contact layer. However the presence of impurities on the sample surface was found to enhance the Schottky barrier height. In order to enhance the electrical performance of the

device, the contact is required to be annealed at 440^{o}C for 1 minute in the JipelecJetfirst 100 RTP(Rapid Thermal Processor). Therefore, titanium can diffuse into the n-contact layer in order to achieve an Ohmic contact. In the case of Ni/GeAu/Ni/Au for n-type GaAs, a relatively lower annealing temperature at 400^{o}C is needed.To emphasize, Cr/Au is used as the contact metal for n-type Si substrate, but there is no annealing required due to gold's extremely fast diffusion in Si, which can damage the structure.

2.6 References

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Chapter 3

1.3-μm InAs/GaAsQuantum-dot Materials and Photonic Deviceson SiliconSubstrates

In this chapter, we report the development ofthe first room-temperature operation of an electrically pumped 1.3-μm InAs/GaAs QD laser epitaxially grown on a Si (100) substrate. Lasing at 1.302μm has been achieved with threshold current density of 725A/cm^2 and output power of ~26mW for broad area lasers with as-cleaved facets at room temperature.

Although Si based light generation, detection and modulation technologies have been extensively investigated, Si based lasers are still considered to be the holy grail of Si photonics, because they present one of the greatest challenges to be realised among all the Si photonic components, and have massive application potential if successful[1]. The integration of III-V lasers with Si technology is the most promising near-term approach[1]. Among III-V-on-Si (III-V/Si) integration approaches, direct epitaxial growth of III-V compounds on Si substrates isthe most desirable approach[6]. But there are severe issues associated with direct epitaxial growth of III-V materials on Si substrates, i.e., the formation of high-density threading dislocations (TDs) due to the lattice mismatch between III-V compounds and Si, and the formation of anti-phase domains (APDs) due to the polar/non-polar nature of III-V/IV system[8]. For conventional III-V/Si quantum-well (QW) devices, any TD or APD propagating through the QWs will become a non-radiative recombination centre, and hence lead to significant decrement of light emission and absorption[9]. In comparison, QDs have low sensitivity to defects and more temperature-independent operation than

QWs[10]. These novel attributes of QD technology are very promising for development of III-V/Si photonic devices by using both MOCVD and MBE. In addition, the optical and electrical properties of InAsQDs epitaxially grown on a silicon substrate have been investigated to evaluate their potential as a material for photodetectors in this chapter.

3.1 Effects of Growth Temperature of the GaAs Nucleation Layer on InAs/GaAs QDs

InAs/GaAs QD samples were fabricated on phosphorus-doped Si substrates with 4^{o} offcut towards [110] plane by solid source MBE. Oxide desorption was performed by holding the Si substrate at a temperature of 900^{o}C for 10 minutes.In the literature, pre-oxidation for creating fresh oxide following by hydrofluoric acid (HF) treatment are recommended. But the HF etchtended to bring additional contaminations, such as carbon based chemicals. The high temperature oxide desorption appears to be the bettersolution to remove the oxide from the Si substrate for us.The Si substrate was then cooled down for the growth of a 30 nm GaAs nucleation layer with low growth rate of 0.1ML/s. The growth of the GaAs nucleation layer was then studied for growth temperatures of 380^{o}C, 400^{o}C and 420^{o}C, respectively. Subsequently, an additional 970nm GaAs layer was grown with a high growth rate of 0.7ML/s at a higher temperature. InGaAs/GaAs dislocation filter layers, consisting of two repeats of a five-fold (10nm $In_{0.15}Ga_{0.85}As$/10nm GaAs) superlattices (SPLs) and 400nm GaAs, were used[8]. Finally 1μm SPL layers of alternating 5nm GaAs/5nm $Al_{0.4}Ga_{0.6}As$ layers completed the III-V buffer layers. Five InAs/InGaAs DWELL layers were then grown at optimized conditions as on GaAs substrates, with each layer consisting of 3.0 MLs of InAs grown on 2nm of $In_{0.15}Ga_{0.85}As$and capped by 6 nm of $In_{0.15}Ga_{0.85}As$[14]. 45nm GaAs barriers separated the five DWELLs. The growth temperature was 580 °C for GaAs, and 510°C for the In-containing layers.

The schematic of epitaxial growth structure is shown in Figure 3.1. The GaAs/AlGaAs cladding layers provide optical confinement to the InAs/GaAs dot-in-a-well (DWELL). The active region QD layers, the GaAs layers and AlGaAs layers were grown at 600^{o}C, respectively. P and N type doping were accomplished with Be and Si, respectively. The dislocation filter is made up of 5 InGaAs/GaAs quantum well layers separated by 100Åthick

of GaAs layers. Furthermore, self-terminating As pre-layer is occupied instead to produce a relatively smooth surface morphology. In the study of As pre-layer, initial As_4 exposure at the GaAs nucleation has significant advantage in surface morphology over As_2 exposure, because As_4 dealt less surface damage in comparison with As_2.

Figure 3.1: Cross-sectional schematic of fabricated InAs/InGaAs dot-in-a-well (DWELL) structure on Si substrate.

Atomic force microscopy (AFM) measurements were performed on uncapped samples in which the growth was halted after the formation of the first-layer InAs QDs. A typical AFM image for the sample with the initial GaAs nucleation layer grown at 400^{o}C is shown in the inset of Figure 3.2, from which a QD density of 4.3 × 10^{10} cm^{-2} is obtained.Figure 3.2compares RT PL spectra of InAs/GaAs QDs grown on Si substrates with different GaAs nucleation temperatures and with a reference QD sample grown on GaAs substrate. The QDs yield RT emission at around 1.3 µm with full width at half maximum (FWHM) of ~30 meV for all the samples shown in Figure 3.2. These PL linewidths obtained from InAs/GaAs QDs on Si substrates are much narrower than that of ~53 meV reported for InAs/Sb:GaAs QDs grown on a Si substrate by MOCVD[15], and it is comparable to the values obtained forGaAs-based 1.3-µm InAs QDs[14].

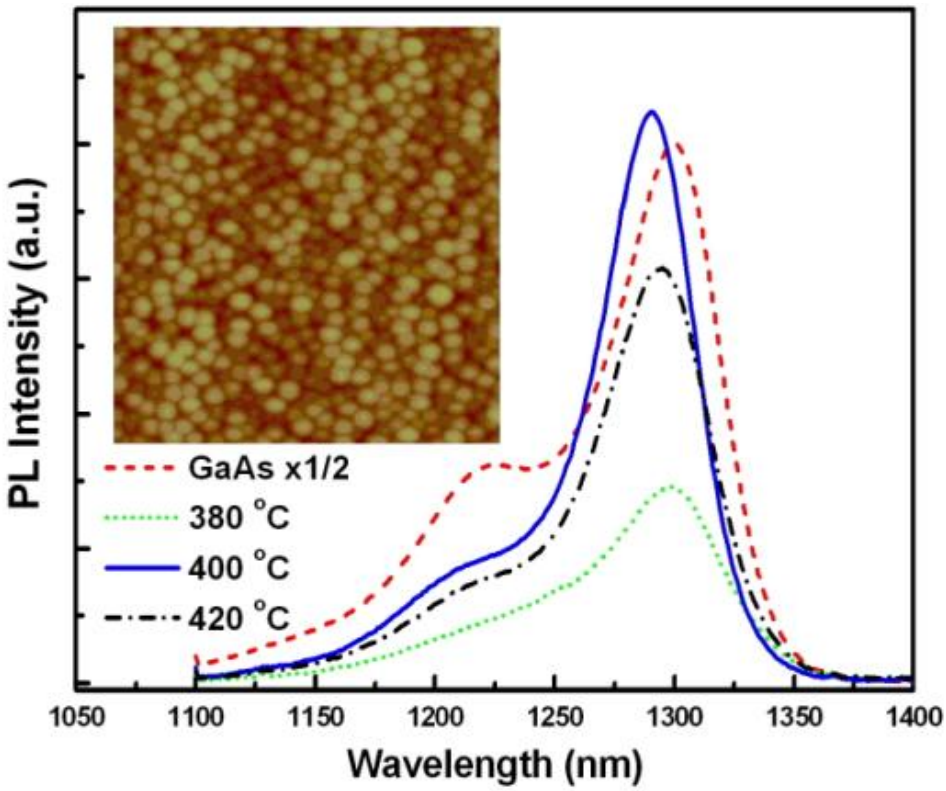

Figure 3.2: Room temperature PL spectra of InAs/GaAs QDs grown on Si substrate with different growth temperatures for the initial GaAs nucleation layer. The room temperaturePL spectrum of InAs/GaAs QDs grown on GaAs substrate is also shown as a reference. The inset shows a 1 × 1 μm^2 AFM image of InAs/GaAs QDs grown on Si substrate.

Of considerable significance is that the PL intensity of the InAs/GaAs QD ground-state transition on Si is strongly dependent on the growth temperature of the initial GaAs nucleation layer. The strongest PL intensity for InAs/GaAs QDs on Si substrate is obtained from the sample with initial GaAs growth at 400 °C, and it is more than a half that of InAs QDs grown on GaAs substrate. It should be mentioned that the InAs QDs grown on GaAs substrate were grown under optimized conditions and represents very high optical quality as the QD laser diode based on identical growth parameters gives an extremely low $J_{th}$of 17 $A/cm^2$and high output power over 100 mWat RT[11].

Single domain GaAs can be epitaxially grown on Si substrate by setting the substrate temperature to a proper value at the beginning of the buffer layer formation, because the surface reconstruction of the first layer on Si varies depending on the temperature at which the Si surface reacts with As. The dislocation density in the GaAs buffer is also very sensitive to the initial nucleation temperature of GaAs, as discussed later. By comparing the PL

spectra of samples with low temperature migration enhanced epitaxy (MEE) at 380°C, 400°C and 420°C, the PL intensity and linewidth plots indicate that 400°C appears to be the optimum growth temperature for the initial GaAs nucleation layers, as shown in Figure 3.2.

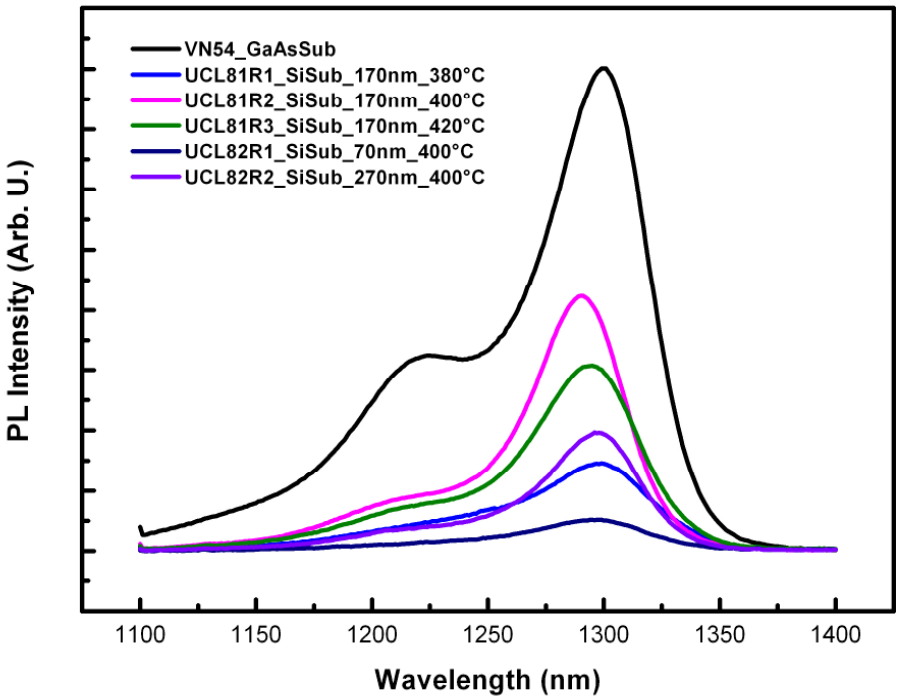

Figure 3.3: Room temperature PL spectra of InAs/GaAs QDs grown on GaAs and Si substrates. For Si substrate, there are five samples with different growth conditions.

Apart from the studies of GaAs nucleation temperature on Si substrate, there are further studies carried on the thickness of initial low-temperature GaAs on Si. In Figure 3.3, the highest PL intensity is obtained from the reference sample VN54 on a GaAs substrate, following by UCL81R2 on Si substrate, which has almost half of the PL intensity of VN54. It has been discussed above that 400°C is the optimum nucleation temperature. UCL81R2 gives the highest PL intensity on Si substrate with a low-temperature GaAs thickness of 170nm at the optimum nucleation temperature, which indicates the optimum thickness of low-temperature GaAs buffer. Thicker and thinner low-temperature GaAs buffer are studied on UCL82R1 and UCL82R2 for comparisons with the same nucleation temperature.It can be observed that there is a strong degradation in PL intensity in UCL82R1, which has a thinner 70nm low-temperature GaAs buffer layer. A thinner low-temperature buffer might ruin the

surface morphology of high temperature GaAs buffer grown above, therefore, further influence the growth of active layers. The thicker 270nm low-temperature GaAs layer (UCL82R2)will also degrade the quality of grown GaAs, as it was grown at lower temperature than optimized temperature for GaAs and thus tends to create additional defects.

3.2 Cross-sectional Transmission Electron Microscopy

To understand the effect of the growth temperature of the initial GaAs nucleation layer on the optical properties of InAs/GaAs QDs on Si substrate, TEM measurements were performed to compare the structural properties of GaAs/Si interfaces with different GaAs nucleation temperatures, as shown in Figure 3.4.

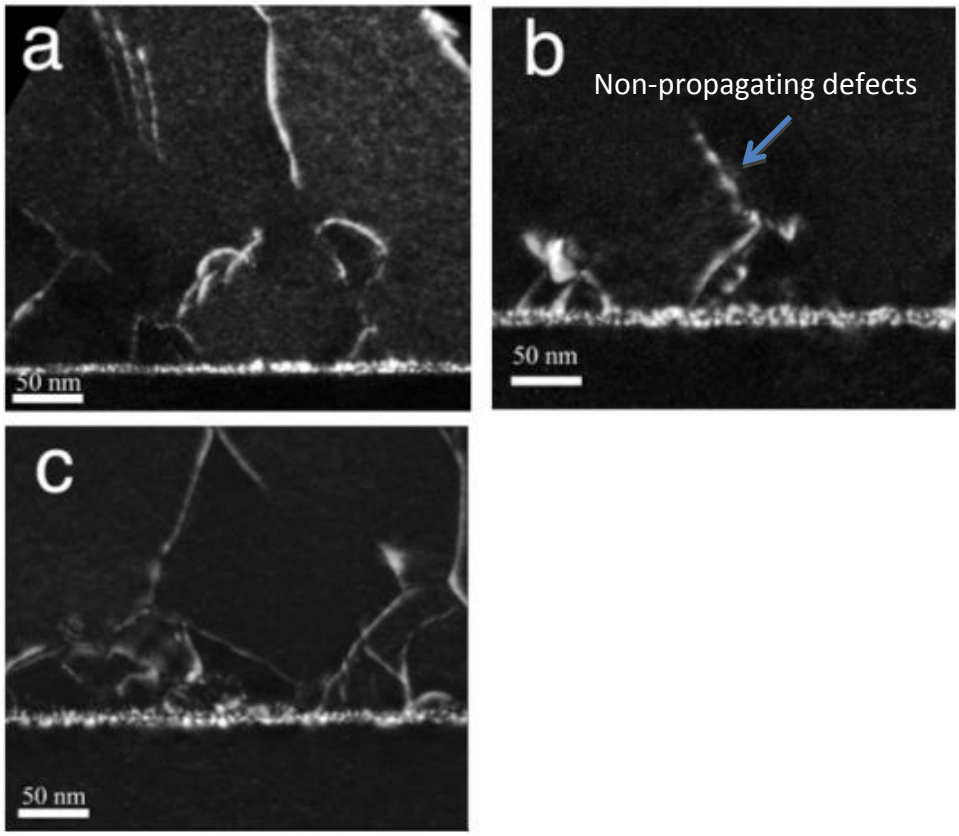

Figure 3.4: Cross-sectional TEM images of epitaxial structures at different nucleation temperature a)380°C, b)400°C and c)420°C.

The defects are generated at the GaAs/Si interface for all the samples shown in Figure

3.4 due to the mismatch between GaAs and Si. Most defects are confined within 50 nm of the GaAs/Si interface while some propagate into the III-V buffer layers. The density of defects propagating into the GaAs buffer is strongly dependent on the GaAs nucleation temperature with the lowest density of defects at 400 °C, and hence the strongest PL intensity for Si-based InAs/GaAs QDs observed in Figure 3.2.

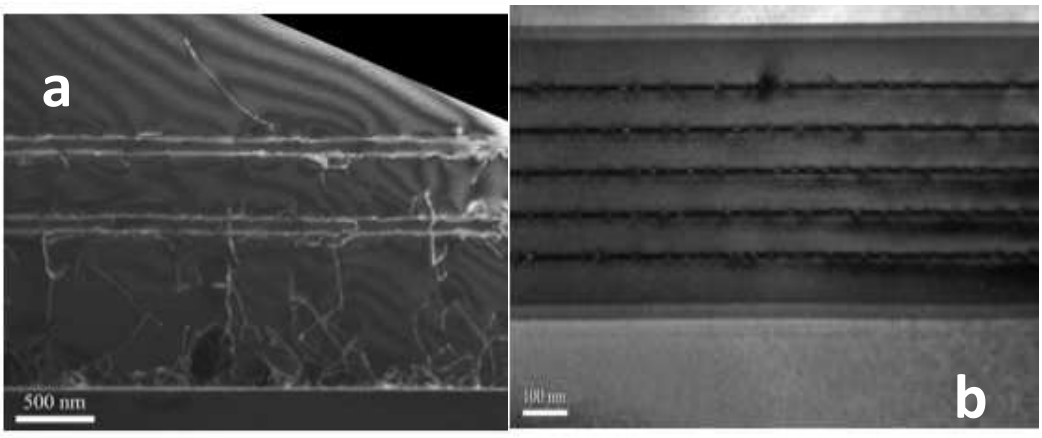

Figure 3.5: TEM images of a) QW dislocation filter layers and b) QD active region.

In case of APDs, there are no APDs observed as shown in Figure 3.4 and AFM images as shown in Figure 3.7. Therefore, TDs appear to be the major type of defects that to be avoided. The TDs can be reduced by occupying InGaAs/GaAs dislocation filters, where it can be observed in Figure 3.5a that approximately 75% of TDs are bent or stopped by the first QW dislocation filter. By growing an additional dislocation filter layer, most TDs are confined beneath this layer, with least influence on the active layers grown above. In addition, there are almost no significant TDs found with the current resolution TEM images of InAs/InGaAs DWELLs as shown in Figure 3.4b. The 5 layers of InAs/InGaAs DWELL structure shown in Figure 3.4b was grown at the center of an undoped 150-nm GaAs/AlGaAs waveguide layer.

3.3 AFM Studies of Surface InAs QDs

In order to examine the growth quality of buffer structures, the AFM images of surface grown InAs QDs are studied here to further verify the results. The surface InAs QD layer is grown on a 2nm InGaAsbuffer layer. The QDs were grown at 510^{o}C with a deposition rate of 0.093ML/s and a total amount of InAsdeposition of 2.79ML.

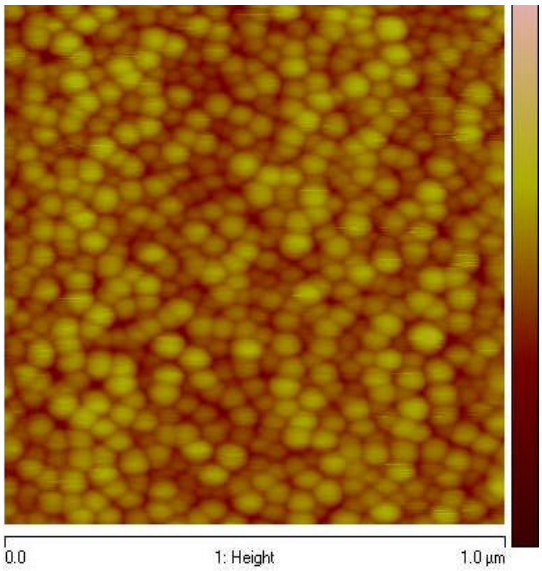

Figure 3.6: 1×1μm^{2}AFM images of uncapped InAs QDs grown on Si substrate.

Figure 3.6 shows an AFM image from the laser test structure in which the growth was terminated immediately after the dot deposition, where the InAs QDs remains uncapped. A dot density of 4.3×10^{10}cm^{-2} is estimated from this image. As we studied the effects of GaAs nucleation temperature and thickness on the PL intensity of InAs QDs, the correspondent AFM images of uncapped InAs QDs under these different growth conditions are also listed in Figure 3.7 to prove the results. It can be clearly observed that there are defected dots existing in the AFM images, which are the accumulated InAs clusters due to strain release. The quantum dots are relatively small to be observed in the 5×5μm^{2}AFM iamges, where only big defect dots can be observed.The defect-dot densities of 5.72×10^8, 2.68×10^8, and 8.28×10^8cm^{-2} were obtained for the sample a, b and c with the initial GaAs layer nucleated at 380, 400, and 420^{o}C, respectively. By occupying the optimum nucleation temperature at 400^{o}C, samples d and e with different thickness of initial low-temperature GaAs (70nm and 270nm) have corresponding defect-dot density of $1.79\times 10^9$and 3.76×10^8cm^{-2}.

Figure 3.7a, b and c show the nucleation temperature optimization, which gives the optimum nucleation temperature at 400^{o}C with the least amount of defected dots. By using the optimized nucleation temperature, the low-temperature GaAs buffer layers are grown with other two different thicknesses are shown in Figure 3.7. The sample in Figure 3.7d with thinnest low-temperature GaAs buffer layer at 70nm has the highest defect-dot density,

which corresponds to the weakest PL intensity in Figure 3.3. The sample in Figure 3.7e with the thickest (270nm) low-temperature GaAs bufferof all has a much lower defect-dot density, but is still higher than the sample in Figure 3.7b with both optimum nucleation temperature (400^{o}C) and thickness (170nm).

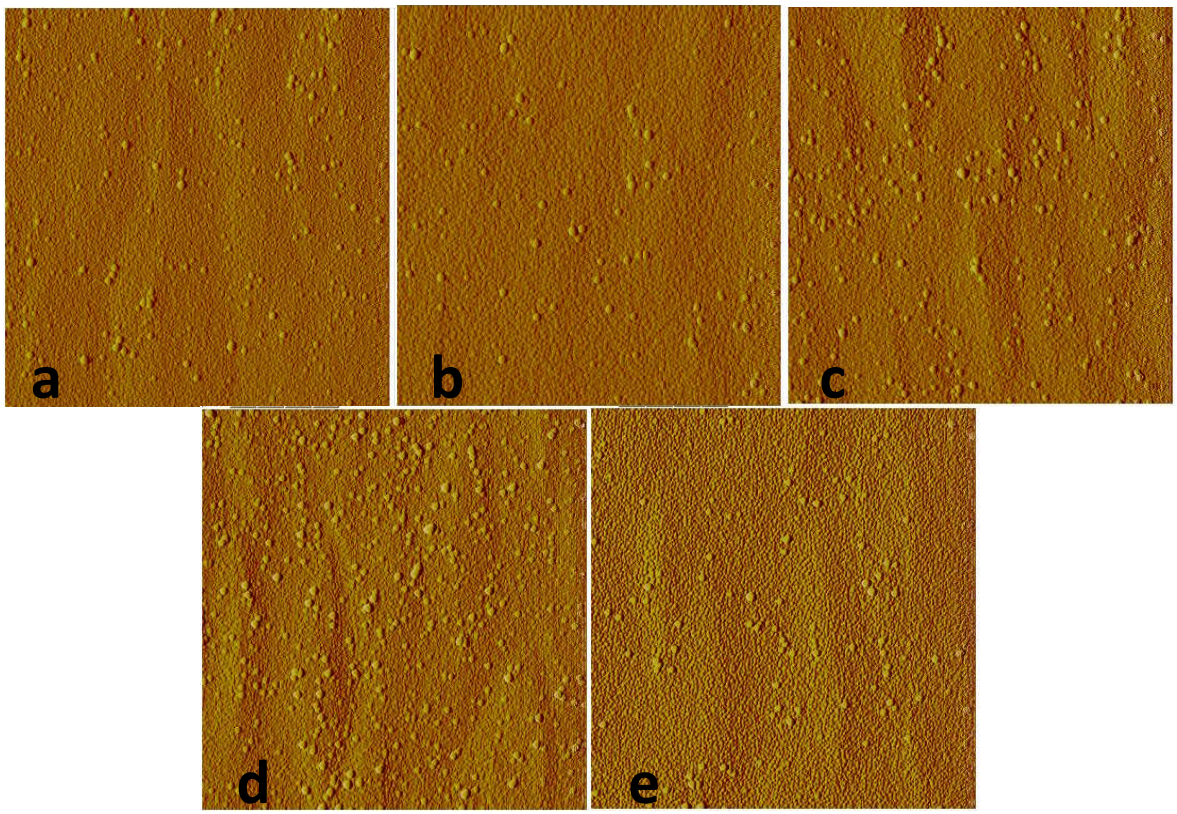

Figure 3.7: 5×5μm^{2} AFM images of surface InAs QDs under different growth conditions. a) 170nm at 380^{o}C, b)170nm at 400^{o}C, c)170nm at 420^{o}C, d)70nm at 400^{o}C and e)270nm at 400^{o}C

The AFM results show a direct correlation between defect-dot density and RT PL intensity, which is strongly dependent on the nucleation temperature and thickness of low-temperature GaAs buffer layer at the GaAs/Si interface. The strongest RT PL occurson the InAs/InGaAs QD sample on Si at 400^{o}C nucleation temperature with 170nm thickness of the buffer layer.

An etch-pit density (EPD) test is introduced to further verify the result as shown in Table 3.1. All three samples are etched 1.5μm down from the surface, where the etchant used for the EPD delineation is a mixture of H_3PO_4, H_2O_2, and H_2O (in a 1:1:3 ratio).From

Table 3.1, it can be observed that the sample grown at 380°C has 1.7 times higher defect-density than the optimised growth at 400°C, where the sample grown at 420°C is even worse with 13.55 times higher. This EPD comparison explains the intensity differences in RT PL correspondently as shown in Figure 3.2. RT PL spectra of all three samples are investigated, excited with a low laser power approximately 5mW. Therefore, it is verified that the defect density within GaAs buffer layers is strongly dependent on the GaAs nucleation temperature. The relative lower temperature at 380°C generates significantly more defected dots than the other two due to its poor material quality and high TD density at low temperature nucleation. At 400°C, the higher temperature has provided atoms with much higher mobility to move around in order to eliminate surface defects. But excess thermal energy can also induce strong atomic movement, and therefore damage the sample surface, which explains the PL degradation at 420°C. Therefore, we can conclude that a low-temperature GaAs buffer layer at 400°C with thickness of 170 nm appears to be the optimum growth condition for strong PL intensity.

GaAs/Si	380°C	400°C	420°C
Etch Pit Density	$1.03\times10^{7}cm^{-2}$	$6.03\times10^{6}cm^{-2}$	$8.17\times10^{7}cm^{-2}$

Table 3.1: EPDs of the laser structures on Si with different growth temperature.

3.4 Temperature Dependent Photoluminescence

Temperature-dependent PL spectra ranging from 10 to 300 K were further studied for all the InAs/GaAs QDs grown on Si substrate. All samples were mounted on a flat copper plate within the cryostat under accurate temperature control. A solid-state laser, emitting at 532nm, was used as excitation source; the emitted radiation from the material is detected by a TE-cooled Ge detector.A ¼m Newport monochromator with a focal length of 260mm is used here. At last, a fixed laser power of 30mW was here used for temperature dependent PL measurements for all samples.

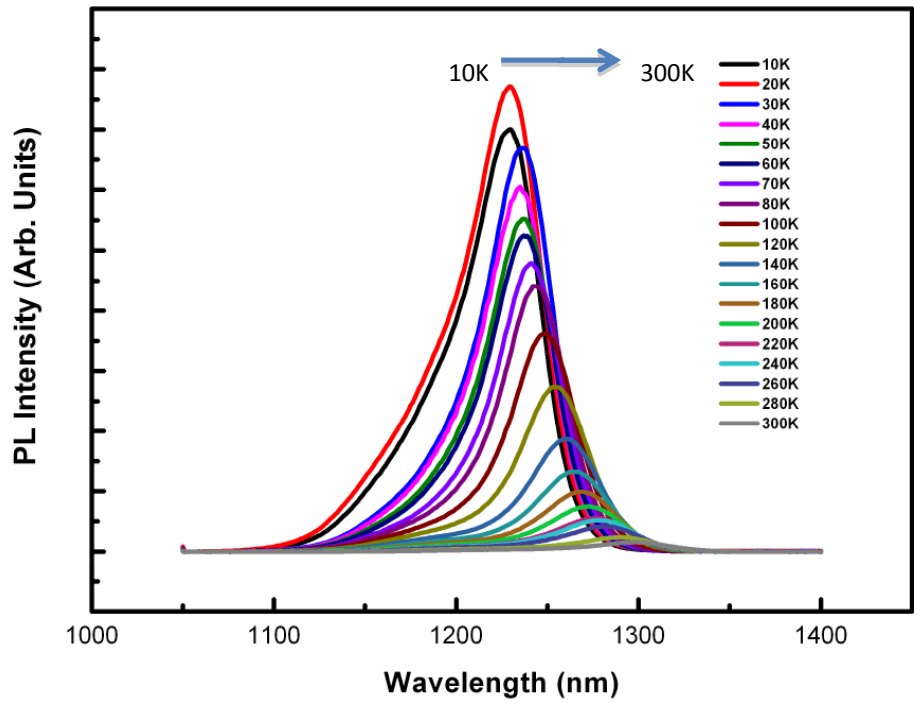

Figure 3.8: Temperature dependent PL spectra ranging from 10K to 300K for InAs/InGaAs QDs grown on silicon substrate.

The PL intensity of Si substrate based InAs/InGaAs QDs is decreasing simultaneously with the rising temperature as shown in Figure 3.8. Because the defect density of InAs/InGaAs QDs grown on Si is significantly higher in comparison with GaAs-based QDs, the carrier trapping and escape are relativelystrong in this case. Therefore, it is possible that even though the carrier confinement become stronger at low temperature,excited state emission can still be hardly observed here. A corresponding blueshift of peak wavelength is also clearly observed in Figure 3.8 with dropping temperature, which is mainly caused by the shrinking of lattice constant with decreasing temperature.To investigate further, Figure 3.9 shows a temperature dependent peak energy plot of five samples with different growth conditions.At room temperature, there are no significant differences among 5 samples in peak energy, but follow an almost linear increment in peak energy with temperature from 300K down to 10K, UCL81R2 with the optimum growth conditions, has the strongest blue-shift in peak energy, whereas samples UCL82R1 and UCL81R1, with much higher defect density,showa relatively weak wavelength shift.

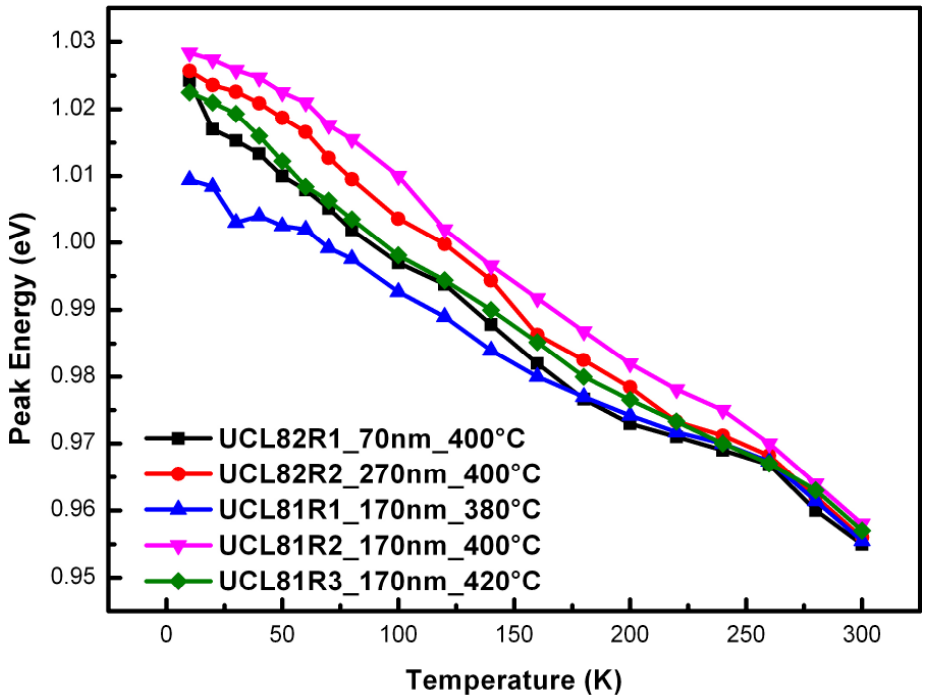

Figure 3.9: Temperature dependent peak energy plots versus increasing temperature ranging from 10K to 300K. QD samples directly grown on Si substrates at different growth conditions are shown above.

There is no exact and explicit explanation to this so far. In general, there is a lift in the band edges of the conduction and valence bands at low temperature, and thus the band gap is widened, so ablue-shift of peak energy occurs. A possible explanation to the differences in the gradients of wavelength blue-shift, as shown in Figure 3.9, is that the samples with high defect density tend to trap carriers beneath the band edge of the conduction band or above the band edge of the valence band, therefore, carrier recombination with lower energy will occur.

3.4.1 Arrhenius Plots of the PL Intensity

In order to further investigate the mechanisms of the influence of temperature and thickness of GaAs nucleation layer on the optical properties of Si-based InAs/GaAs QDs, the integrated PL intensity(IPLI)between 10 and 300 K was analyzed. With a low laser power excitation, only ground-state emission was present in the PL. Figure 3.10 shows the Arrhenius plot of the IPLI for three different growth temperature of GaAs nucleation layer.

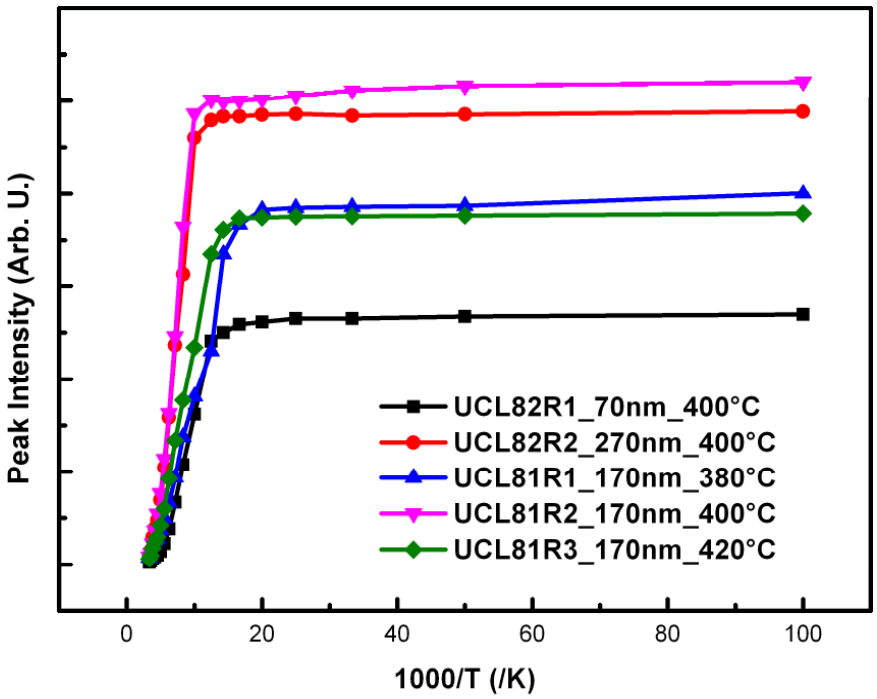

Figure 3.10: Arrhenius plots of the IPLI of InAs QD samples on Si with three different nucleation temperatures at 380°C (blue), 400°C (pink) and 420°C (green) in case of 170nm thick low-temperature GaAs buffer. Arrhenius plots of the IPLI of InAs QD samples on Si with two different low-temperature GaAs buffer layer thickness of 70nm (black) and 270nm (red) both at 400°C.

In a physical model, these temperature-dependent variations of IPLI could be understood in terms of the recombination rates and the geometric dimensions of the dots. The IPLI of UCL81R2 and UCL82R2 remain almost constant from 10K to 77K, and then decreases gradually until RT. These two samples are grown at the same nucleation temperature of 400°C, but with different low-temperature GaAs thicknesses of 170nm and 270nm. UCL81R2, with optimum growth condition, has shown the strongest IPLI all over the whole temperature range, following by UCL82R2.Although the IPLI starts dropping dramatically above 77K, the IPLI still remained persistent at a high level, which is attributed to the increase in oscillator strength due to additional lateral confinement in QDs compared to conventional quantum wells. In addition, the percentage of change in the energetic position of PL peak emission remains small below 77K. The reduction in IPLI is normally

attributed to thermal escape into the barrier material following by non-radiative recombination in the barrier. Therefore, in this case, the IPLI differences among three samples are mainly caused by the defect density difference due to the nucleation temperature. Clearly, the sample grown at 400^{o}Cwith 170nm thick low-temperature GaAs buffer layer has the least amount of TDs, which gives the highest IPLI over the temperature range from 10K-300K.

Note that the IPLI has a quenching threshold temperature for all samples. It can be observed in Figure 3.10 that InAs/GaAs exhibits thehighest quenching temperature of 77K for the optimised growth at 400^{o}C, which indicates less thermal escape caused by the reduction in defect density. The optimized sample at 400^{o}C has a much lower defect density than both higher and lower growth temperature.Hence, the carrier lifetime in the barrier is longer, which explains the persistence of IPLI to a higher temperature. It can be clearly observed that the quenching occurs due to the losses in the barrier at higher temperature. The IPLI start to quench at the point where the carrier capture time into QDs is getting longer than the carrier lifetime in the barrier, which indicates that there are more carriers escaped than captured. Here, the carrier lifetime in the barrier is strongly dependent on the non-radiative recombination centre, i.e., the concentration of defects. Therefore, the high quality growth of GaAs buffer layer at 400^{o}C nucleation provides a much higher carrier lifetime in the barrier material, leading to the highest room temperature IPLI among three samples.

Additionally, to have a clearer view of temperature sensitivity of PL intensity for samples with five different growth conditions, Figure 3.11 shows the peak PL intensity versus temperature. It can be observed that the peak PL intensity of UCL81R2 rises sharply with decreasing temperature from 300K. Samples with higher defect density as described above, have flatter increment with dropping temperature, especially in the case of UCL82R1, which has the highest defect-dot density of 1.79$\times$ 10^{9}cm^{-2}. This result indicates that the carrier recombination of QDs is strongly dependent on defected dot density. Therefore, the most efficient carrier recombination at 10K is observed from UCL81R2 with smallest amount of defected dots, which has the highest peak PL intensity of all.

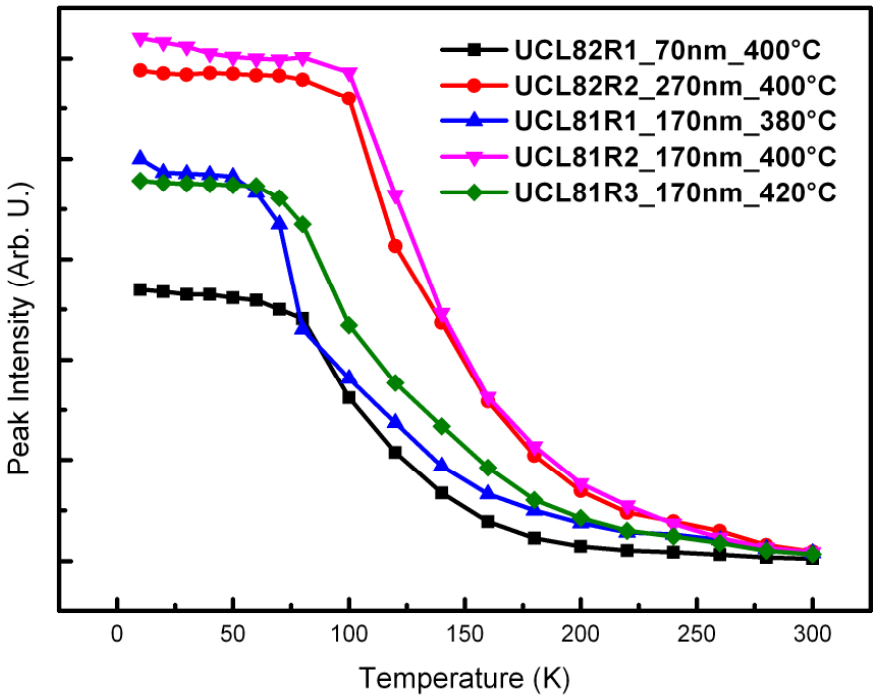

Figure 3.11: Peak PL intensity versus temperature of InAs QD samples on Si with three different nucleation temperatures at 380°C (blue), 400°C (pink) and 420°C (green) in case of 170nm thick low-temperature GaAs buffer. Peak PL intensity plots versus temperature of InAs QD samples on Si with two different low-temperature GaAs buffer layer thickness of 70nm (black) and 270nm (red) both at 400°C.

3.4.2 FWHM Plots of the Temperature Dependent PL

It can be observed from Figure 3.12 that the FWHM of the PL spectrum varies between 33meV to 37meV for sample grown at 400°C in the entire temperature range from 10K to 300K, which has the least variation of 12% and narrowestroom-temperature linewidthamong all samples. In comparison, samples grown at 380°C and 400°C have relatively larger variations of 20% and 25%. The reference sample grown on GaAs substrate has the strongest FWHM variation for temperature dependent PL, because the appearance of the emission from small QDs at low temperatures (below 200K) has broadened the FWHM of the spectrum. At room temperature, a relatively narrow linewidth of 36.69meV is still observed for the reference sample on a GaAs substrate, while the sample grown at

400°C (UCL81R2) shows the narrowest linewidth of 33.22meV. Both samples (UCL82R1 and UCL82R3) grown at 380°C and 420°C have broader linewidth at 39.28meV and35.77meV. Such a small variation in the FWHM of the PL emission indicates the uniformity of QD sizes for the sample grown at 400°C.

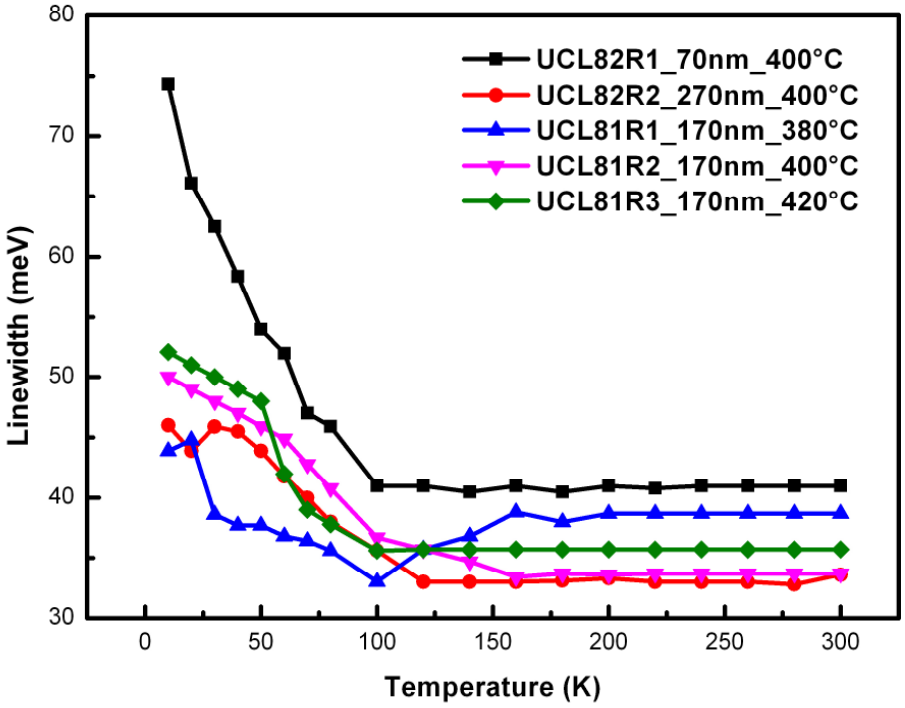

Figure 3.12: PL linewidth (FWHM) versus temperature plot for InAs QD samples on Si with three different nucleation temperatures at 380°C (blue), 400°C (pink) and 420°C (green), including two additional reference sampleswith different low-temperature GaAs thickness of 70nm (black) and 270nm (red).

By having the optimum nucleation temperature at 400°C, UCL82R1 with a thinner 70-nm GaAs buffer has the broadest linewidth of 41.98meV at RT. UCL82R2 with thicker 270-nm GaAs buffer shows a very narrow linewidth similar to UCL81R2. Therefore, in the comparisons of FWHM of PL spectra, UCL81R2 and UCL82R2 with the same nucleation temperature, but different thickness of low-temperature GaAs buffer at 170nm and 270nm respectively, have similar performance in FWHM optimization.

3.5 Laser Characteristics

Broad-area 50-μm wide stripe lasers with cleaved facets were then formed by applying Ti/Au on the top and Cr/Au on the bottom of the structure. Devices of 3-mm length were bar-tested, being directly probed without any mounting and bonding. For conventional InAs/GaAs QD lasers on GaAs substrates, Ni/GeAu/Ni/Au were used for N-type metal contacts, which provides a low N-contact resistance. Due to the large work function difference between Si and nickel, an alternative metal system has to be selected to produce an Ohmic contact. Aluminum was first selected as the N-contact metal on the Si substrate.

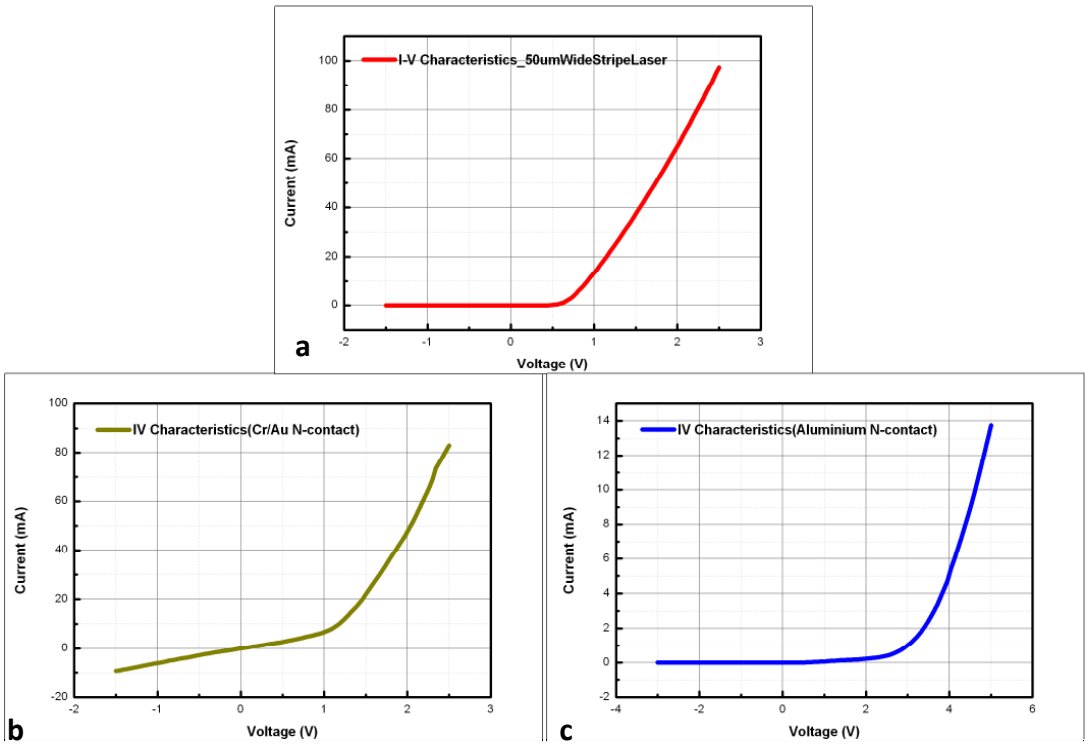

Figure 3.13: I-V characteristics of a) series resistance of the laser bar, b)Cr/Au N-contact resistance and c)Aluminium N-contact resistance.

One additional reason of using Cr/Au is that Au diffuses strongly within Si, and can further destroy the entire device. Note that Au is forbidden in Si processing industries. From Figure 3.13c, the Al N-contact on Si has an extremely high contact resistivity ~7×10^{-4}Ohm/cm^2. To compare, in Figure 3.13b, using Cr/Au instead induces a much lower contact

resistivity ~5×10^{-5}Ohm/cm^2, as Cr has a similar work function to N+ Si. Figure 3.13a shows the series resistance of 50um wide stripe laser made by improved Cr/Au N-contact at 17.8Ohm. There is 20nm thick Cr deposited first before the Au evaporation, in order to prevent possible Au diffusion into Si substrate.

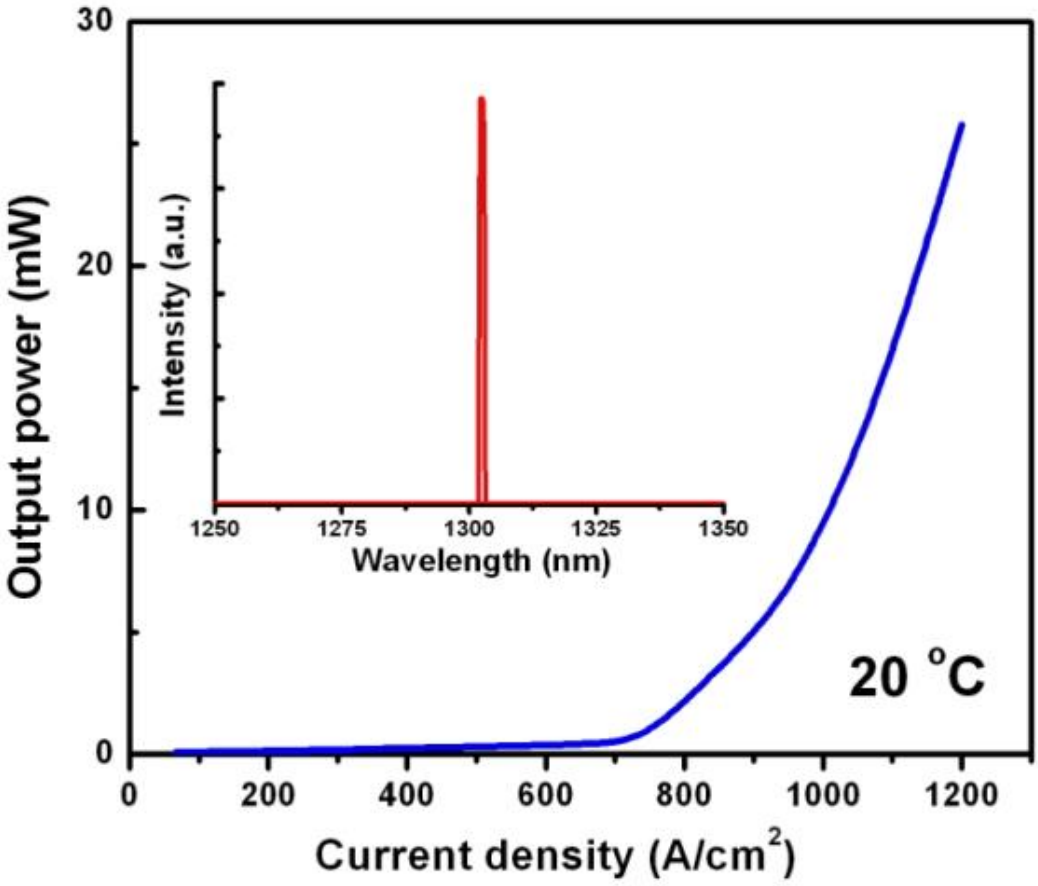

Figure 3.14: Room-temperature Light output against current for Si-based InAs/GaAs QD laser diodes. The inset shows emission spectra of 5-layer Si-based InAs/GaAs QD laser for different drive currents below and above threshold.

Figure 3.14 shows the light output against current density characteristics of a fabricated device at RT. Laser characteristics were measured in pulsed mode using a pulse width of 0.1μs and duty cycle of 0.01%. The measured output power is 26mW at an injection current density of 1.2 kA/cm^2, with no evidence of power saturation up to this current density. The RT $J_{th}$is 725 A/cm^2, which is lower than the previously reported values of 900 A/cm2 for a 1.02μm InGaAs/GaAs QD laser directly grown on Si substrate. Note that this

device was processed with as-cleaved facets. The use of high-reflection (HR) coating on the facets in future studies will further decrease J_{th}. The inset in Figure 3.14 shows the laser optical spectrum above threshold, in which RT lasing at 1.302µm is observed.

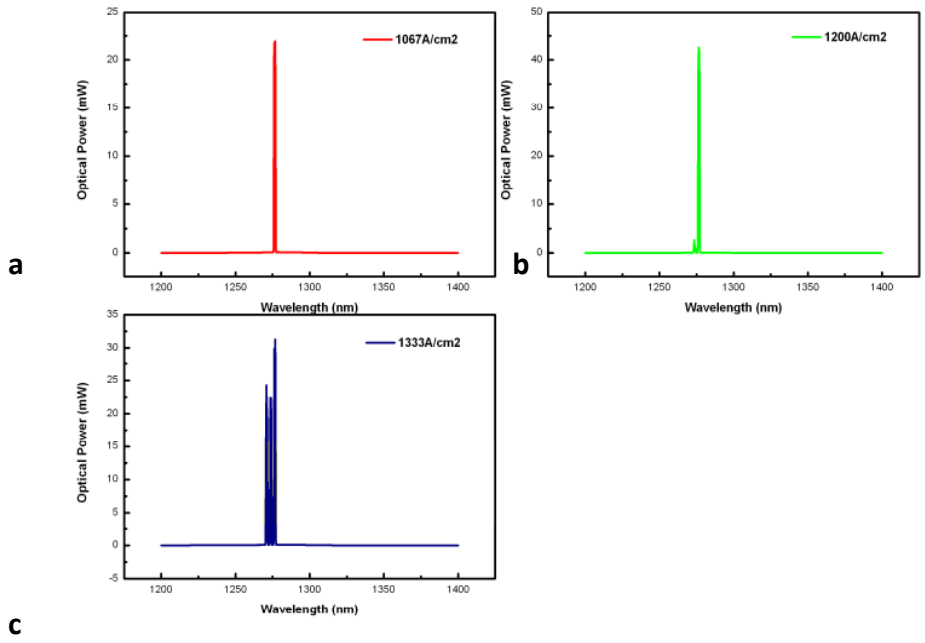

Figure 3.15: Power dependent spectraanalysis. a)1067A/cm^2, b)1200A/cm^2 and c)1333A/cm^2.

There is an extra set of samples with shorter lasing wavelength, which remains to be used for power dependent spectra analysis as shown in Figure 3.15 With an increasing injection current from 1067 A/cm^2 to 1333 A/cm^2, the laser changesfrom single mode to triple mode, while at an intermediate injection current of 1200A/cm^2, it operates as a bi-modal laser. This indicates a good current and optical confinement of the laser device in case of material and cavity qualities, where there is a transition of carriers from a group of dots to the others. Therefore, excess power is converted into additional mode operations.

Figure 3.16 shows the output power for a Si-based InAs/GaAs QD laser at various operation temperatures, ranging from 20 °C to 42 °C. The laser output power starts to roll over above 48^{o}C (not shown in Figure 3.16) due to strong heat generation within the

device.This QD laser has a 42 °C maximum lasing temperature with a characteristic temperature $T_0$of 36 K (Figure 3.17). Note that generally 1.3-µm InAs/GaAs QD lasers show poor T_0in the range of 35 K - 60 K around RT[17]. Characteristic temperature is the parameter that determines the feature degradation of the laser diode, which can be evaluated from L-I dependency (the gradient of threshold current changes with increasing operation temperature) from 20°C to the highest operation temperature.

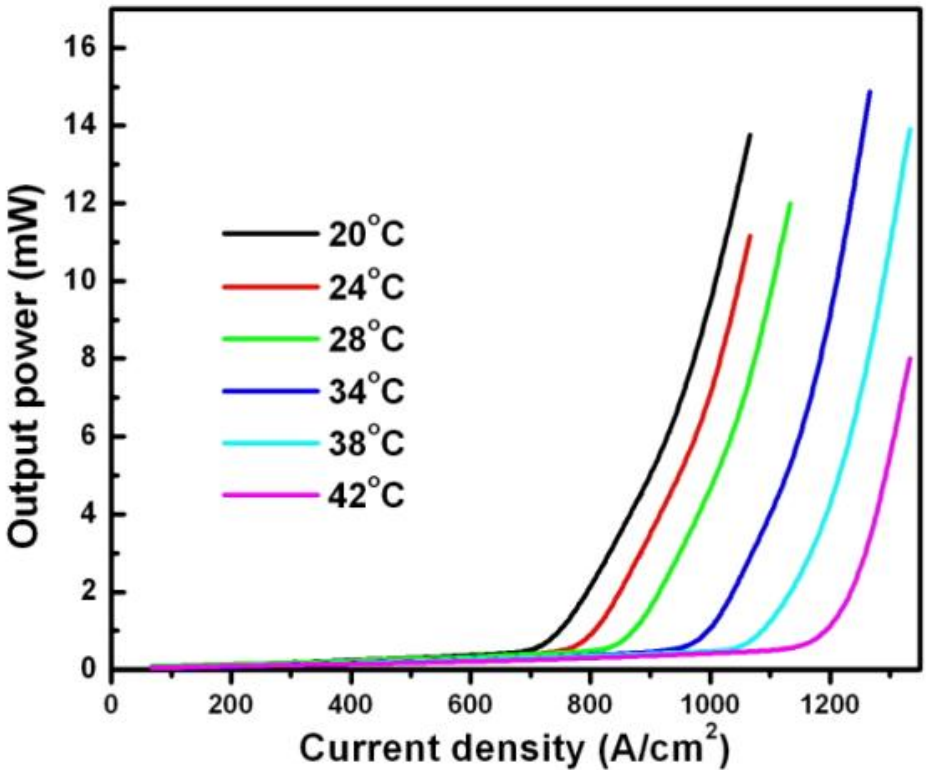

Figure 3.16: Temperature dependent L-I curves from 20°C to 42°C

With the current device, the threshold current density increases exponentiallywith rising operational temperature from 20°C to 48°C as shown in Figure 3.17. The temperature stability of 1.3-µm InAs/GaAs QD lasers on Si could be significantly enhanced by using p-type modulation doping of the QDs, which is a well established technique for dramatically increasing the value of T_0, even up to T_0~∞for GaAs-based QD lasers.The laser device has appeared to be relatively sensitive to the operational temperature changes due to the huge amount of heat generated from the defects at theGaAs/Si interface, as the current is passing through the high-resistance buffer layers.

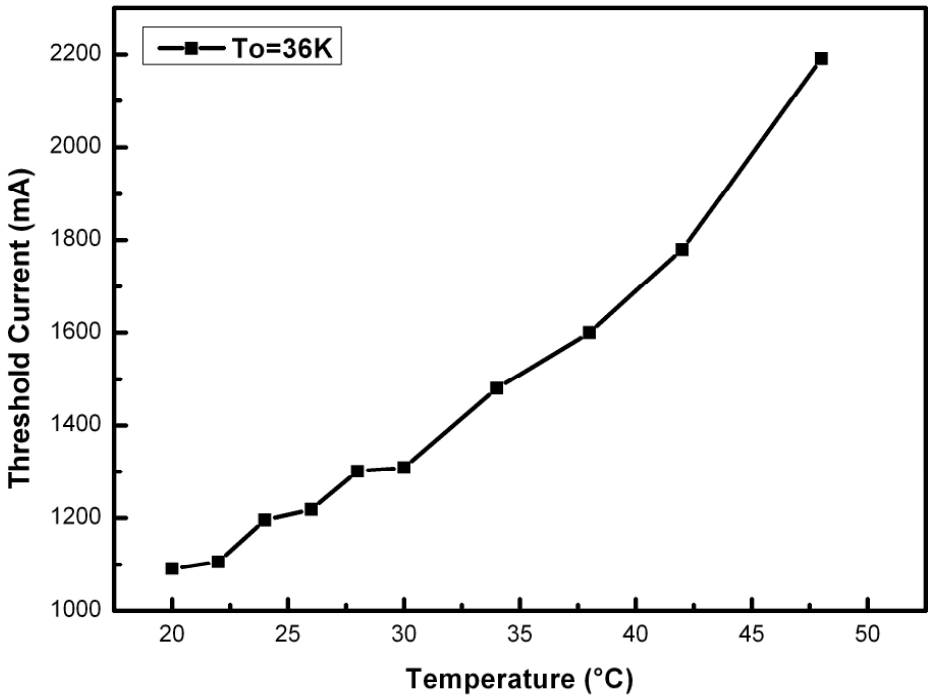

Figure 3.17: Plot of threshold current versus temperature from 20°C to 48°C with a characteristic temperature of 36K.

To summarize, we have demonstrated the first room-temperature operation of 1.3-μm InAs/GaAs QD lasers epitaxially grown on Si substrates by molecular beam epitaxy. The GaAs nucleation temperature on the Si substrate has been first optimized for obtaining high PL intensity of 1.3-μm InAs/GaAs QDs grown on Si substrates. Room-temperature lasing at 1.302 μm has been achieved with an output power of ~26 mW and $J_{th}$of 725 A/cm^2 for a five-layer InAs/GaAs QD device on Si substrate with as-cleaved facets. This study is an essential step toward the monolithic integration of long- wavelength InAs/GaAs QD lasers on Si substrates, as well as for the creation of other III-V devices on Si platform.

3.6 InAs/GaAsQDPhotodetector Grown on Silicon

Silicon based photonic devices have attracted considerable attention over recent years due to the potential to have optical components which are compatible with Si based CMOS circuitry[19]. A number of developments have been made over recent years in the development of Si-based waveguides[20]and modulators[21]. For operation at the

important telecommunications wavelength of 1.3 µm the best on-Silicon infrared detectors are based on growing Ge on Silicon[22]. However these devices suffer from high dark currents, (for example 5 A/cm^2 for operation at 1300nm[22] and 0.1 A/cm^2 for operation at 1500 nm[23], both with a reverse bias of only 1 V, limiting their sensitivities and hence ability to detect low light levels.

Recently great progress has been made at growing InAs QDs on silicon and Ge substrates[24], to realise lasing at a wavelength of 1.3 µm[25]. The Quantum Confined Stark Effect (QCSE) has previously been investigated in In(Ga)As QDs grown on GaAs substrates leading to the idea of using such dots to form tuneable photodetectors[26]and optical modulators[28]. QDs offer several advantages over current Ge on Si based systems due to expected lower dark currents, decreased temperature sensitivity and more tuneability over the operational wavelength. Despite these potential advantages, to date little work has been done to investigate the properties of In(Ga)As QDs grown onto silicon substrates for detector and modulator based applications.Here, we investigate the use of InAsQD structures monolithically grown on silicon as photodetectors. We evaluate the dark current and absorption properties of the QD structures as well as showing the possibility to enhance the signal via avalanche gain at wavelengths beyond the band gap of both silicon and GaAs. We also discuss the possibility of using such structures as optical modulators at wavelengths around 1.3 µm by exploiting a combination of carrier multiplication and QCSE.

3.6.1 Growth and Experiment Details

InAs/GaAsQDs were grown by Molecular Beam Epitaxy on silicon substrates and then fabricated into mesa diodes with optical access. The epitaxial structure is identical to the laser structure except that the thick cladding layers are removed to allow the transmission and absorption of input light, as shown in Figure 3.18. Briefly, the structure comprises a 1.2 µm GaAs buffer layer followed by a 50-period undopedAlGaAs/GaAssuperlattice. A 180 nm N-doped AlGaAs layer was then deposited with a doping concentration of 1x10^{18}/cm^2, which was followed by an intrinsic region consisting of another AlGaAs/GaAssuperlattice then 5 InAsQD layers each separated by a 58 nm GaAs spacer layer. A 180 nm P-doped AlGaAs layer with a doping concentration of 5x10^{18}/cm^2 was then deposited. This was capped witha 200 nm P-doped GaAs layer. Circular mesas with radii of 200, 100, 50 and 25 µm were formed

via wet chemical etching and depositing a top p-contact of Au-Zn-Au and a bottom contact of InGe/Au.

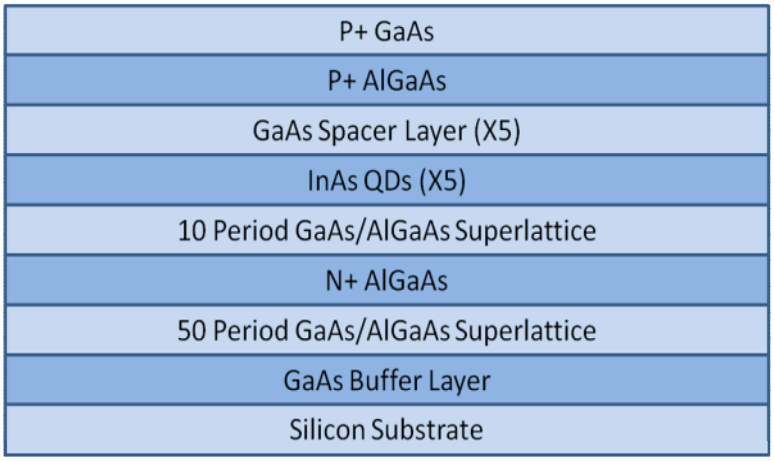

Figure 3.18: InAs/GaAs QD photodiode on Si substrate.

All measurements were performed at room temperature and by directly probing the devices. Forward and reverse bias currents were measured using an Agilent B1500 parametric analyser. Responsivity spectra were determined by measuring the photocurrent through phase sensitive detection where white light was passed through a monochromator and focused onto the mesas and calibrating for the incident power. For avalanche gain measurements the total photocurrent was measured with phase sensitive detection using either a 1064 or 1300 nm laser. The primary photocurrent was extrapolated to high bias and removed from the total signal to yield the avalanche gain. For photoluminescence spectra, the samples were excited with a 532 nm CW laser with a variable output power of up to 1 W, the subsequent emission was then dispersed through a monochromator and measured with a cooled InSb detector.

3.6.2 Results and Discussions

The measured dark currents for diodes with a range of radii are shown in Figure 3.19. The current densities of different sized diodes are in good agreement indicating that the measured dark current is comprised of bulk currents. At low voltages the measured dark current is approximately two orders of magnitude higher than commercially available InGaAs photodiodes. However these values are below those that have been reported for Ge

on silicon devices covering the same spectral range. A sharp increase in the current can be seen around 25 V, this is likely to be due to avalanche multiplication caused by impact ionisation of carriers in either the GaAs barrier layers or the AlGaAs/GaAs grading superlattice.

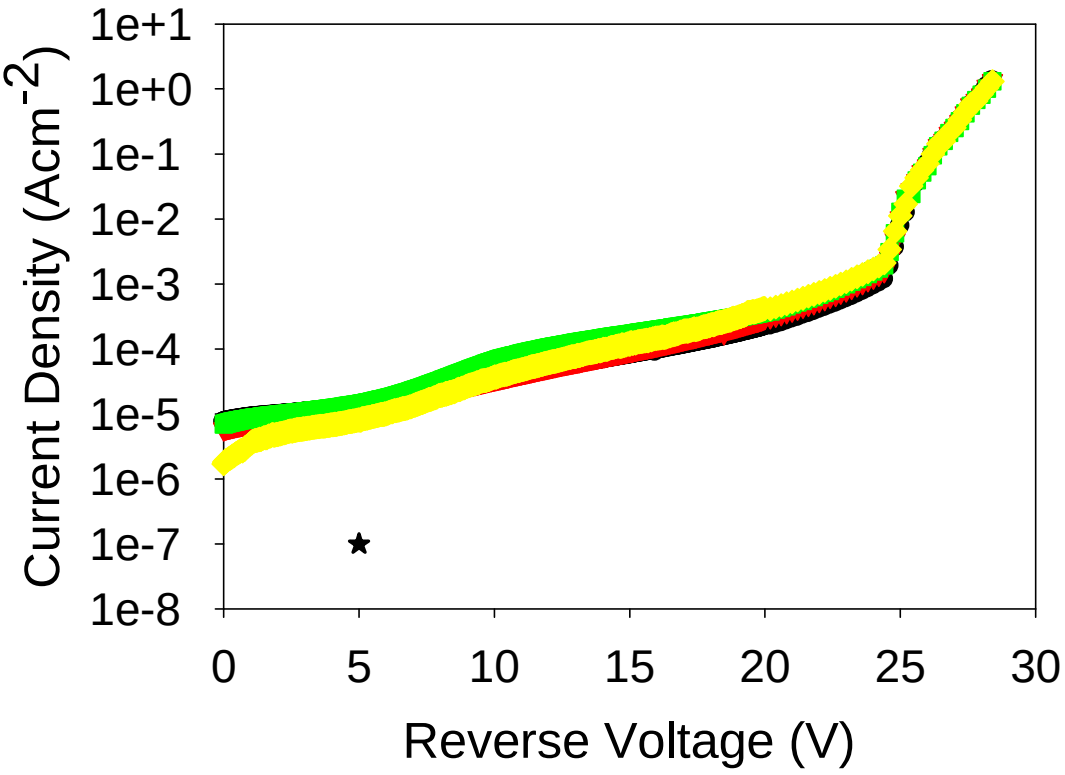

Figure 3.19: Dark current densities for 200 µm (black), 100 µm (red), 50 µm (green) and 25 µm (yellow) radius devices, the star shows the value for a commercial Hamamatsu InGaAs photodiode.

The i-region consists of a 100 nm GaAs/AlGaAs superlattice and 5 periods of QDs separated by 58 nm GaAs spacer layers. A 290 nm thick GaAs layer would give a breakdown voltage of approximately 12 – 15 V[29]. In AlGaAs/GaAs structures it is known that the breakdown properties tend towards that of an equivalent alloy[30], so we attribute the increase in the breakdown voltage observed here to the impact ionisation occurring in both the GaAs spacers and GaAs/AlGaAs superlattice. At voltages above 27 V the current density appears to be limited by series resistance effects; this conclusion is supported by the forward current measurements, where a similar roll off in the current was observed.

To evaluate InAs QDs grown on silicon as a photodetector operating at 1.3 μm we have measured the responsivity of the device, which is shown in Figure 3.20, along with the room temperature photoluminescence (PL) spectra.

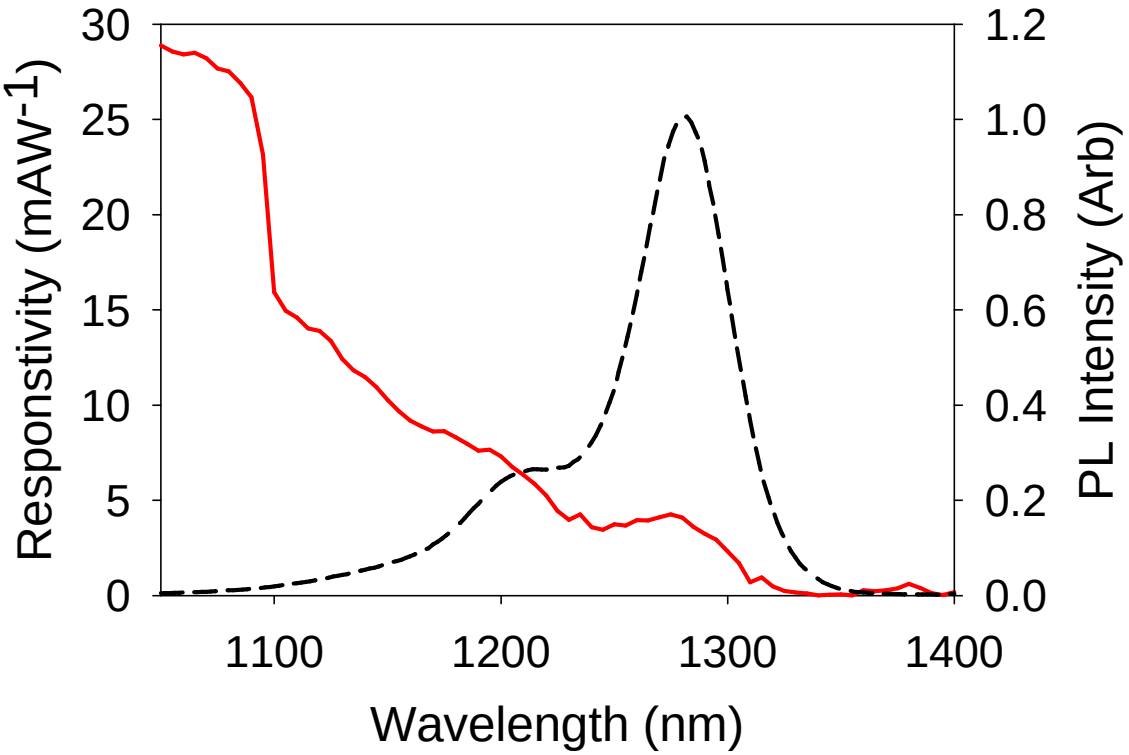

Figure 3.20: Responsivity from a 200 μm radius device. The dotted line shows the photoluminescence spectra.

Emission and absorption from the ground state transition of the QD can be observed with a peak at 1280 nm and a corresponding responstivity of 5 mA/W. A shoulder in the PL is also observed at a wavelength of 1210 nm, although there is not a clear corresponding feature in the absorption at this wavelength. From power dependent PL measurements the relative heights of these two peaks is approximately constant suggesting that there is a bi-modal dot distribution. There is a sharp transition observed in the absorption spectra at 1100 nm in Figure 3.20. Due to the strong absorption but lack of emission in the PL spectra at these wavelengths we attribute this to the wetting layer.

While the responsivity from the ground state of the dots is less than that which has been reported for Ge grown on Siat these wavelengths, it is worth remembering that as we only have 5 layers of dots not all the light at these wavelengths will be absorbed, hence

limiting the responsivity. Although the peak responsivity from the QDs occurs at 1280 nm, overlayed on the responsivity of the GaAs substrate, with only a small absorption tail extending to 1.3 μm, this can be increased in future by refining the growth conditions to give the peak at the desired wavelength. This could be achieved by a number of routes for example by changing the amount of InAs deposited for the dots to form from.

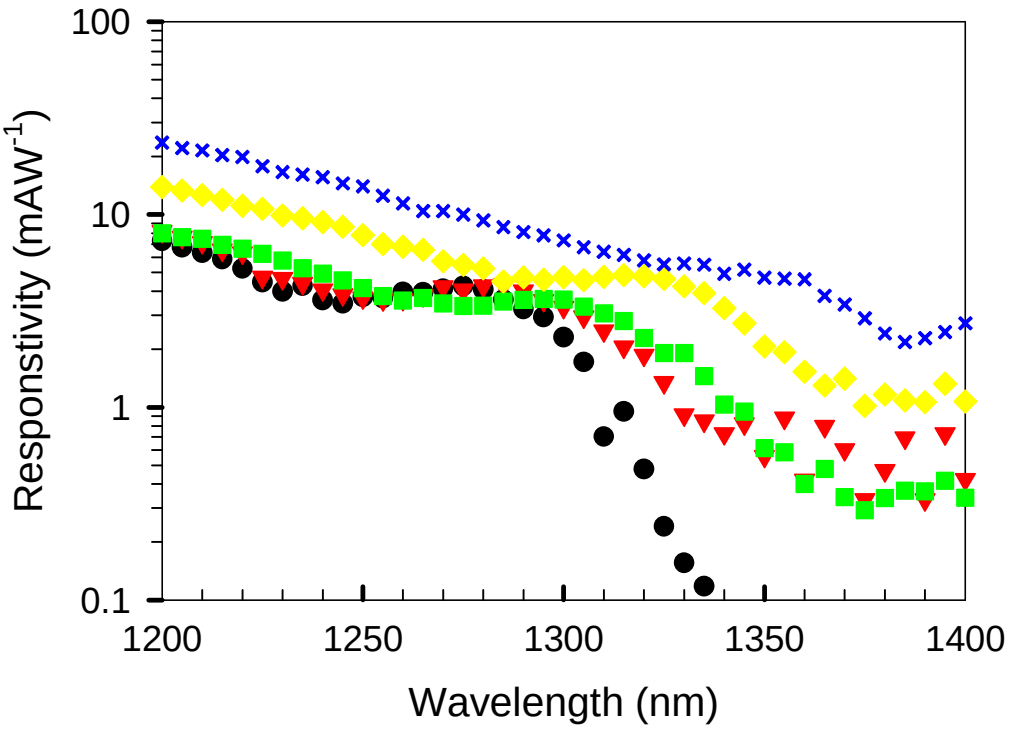

Figure 3.21: Responsivity curves from a 200 μm radius device at reverse biases of 0 V (circles), 5 V (triangles), 10 V (squares), 15 V (diamonds) and 20 V (crosses).

It has previously been shown that that the QCSE can be exploited to shift the absorption wavelength in In(Ga)As QDs [27] grown on GaAs. Shifts in the absorption wavelength of around 30 meV for electric fields varying from 0 to approximately 300 kV/cm [27]have been previously observed offering the possibility of tuning the detection wavelength and forming an optical modulator. To investigate if similar effects are observed in our QDs grown on silicon substrates we have measured the responsivity as a function of reverse bias. The spectra at selected biases are shown in Figure 3.21.

A clear shift in the peak of the QD transition from 1280 nm at 0 V bias to 1360 nm at 20 V can be observed, corresponding to an energy change of 64.2 meV. This value is larger than the 30 meV reported previously for In(Ga)As QDs grown on GaAs [26]because we have

used a larger electric field of 515 kV/cm. For a comparable electric field, we also observed a peak shift of 33 meV, which is consistent with these previous studies.

In addition to a red shift in the absorption with increasing reverse bias, there is an increase in the responsivity as the bias is increased above 10 V. We attribute this to carriers being generated in the QDs and then undergoing impact ionisation and multiplying in the GaAs barriers, as was suggested by the breakdown behaviour observed in Figure 3.19. To investigate this further we have measured the multiplication from the device at wavelengths of 1064 and 1300 nm. These wavelengths were chosen as they are beyond the absorption cut off of GaAs ensuring that the absorption occurs within the wetting layer or the dots themselves.

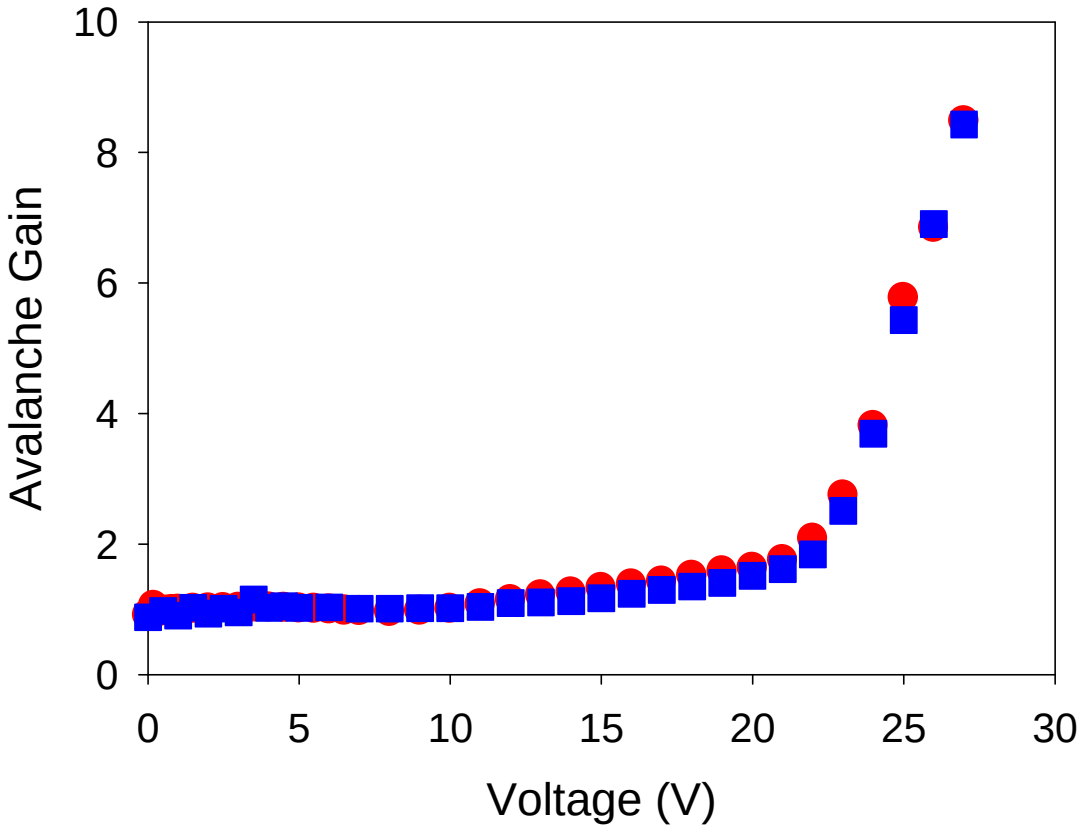

Figure 3.22: Avalanche gain from a 200 μm radius mesa at a wavelength of 1064 nm (circles) and 1300 nm (squares).

Figure 3.22 shows that carriers generated at both 1064 and 1300 nm undergo similar multiplication behaviour. A gradual increase in the multiplication sets in at around 10 V and continues until around 22 V where a more dramatic multiplication occurs. The initial

increase agrees with the increase in responsivity observed in Figure 3.21, while the more abrupt breakdown corresponds with that seen in the dark current in Figure 3.19. Although the large electric field across the structure will result in a red shift of the GaAs absorption edge due to the Franz-Keldsh effect and therefore have a potential influence on the avalanche gain at 1064 nm, the strong agreement with the multiplication at an excitation wavelength of 1300 nm indicates that the behaviour observed in Figure 3.22 is due to absorption in the QDs and subsequent multiplication in the GaAs barriers.

The results in Figure 3.21 and 3.22 show that from a combination of the QCSE and impact ionisation, as the reverse bias is increased the photocurrent at a fixed wavelength increases. These results suggest that In(Ga)As QDs offer a route to develop optical modulators, photodiodes and APDs operating at a wavelength of 1.3 μm grown on silicon substrates.

A key figure of merit for a modulator is the extinction ratio. This is the difference between the off and the on signal. Optical modulators are typically incorporated into a waveguide structure to maximise the absorption. However, due to the device geometry used in this work such a measurement has not been possible. However, from looking at the change in the gain-normalised responsivity with increasing bias we can estimate the potential for this structure as an optical modulator. For a wavelength of 1.3 μm an increase in the responsivity of 2.9 can be observed as the voltage is increased from 0 to 20 V. If this increase in responsivity can be directly transferred to the change in the power generated in an optical modulator, a maximum excitation ratio of 4.7 dB could be achieved. This value is reasonable when compared to that of other on-silicon modulators operating at 1.3 μm of 4.2 dB[32]and at 1.55 μm of 8.1 dB [33]. The highest previously reported extinction ratio at 1.3 μm on InAs QDs grown on GaAs is 13 dB[34], however this device had an optimised absorption spectrum for operation at this wavelength.

There is much room for improvement on our value as the absorption of the dots is not currently optimised for 1.3 μm and if we evaluate the change in responsivity at 1.36 μm (the peak wavelength of the QDs at a bias of 20 V) a maximum extinction ratio of 22.5 dB is predicted. Additionally, we have only predicted the possible use as a modulator up to a voltage of 20 V (before the onset of avalanche gain in Figure 3.21). If the voltage were

further increased we could expect a greater change in the power within a modulator due to the influence of impact ionisation.

In conclusion, we have evaluated the potential of In(Ga)As QDs grown on silicon as photodetectors by characterising their electrical and optical properties. We have found that the structure has fairly low dark currents and have measured absorption from the dots at 1.3 μm. We have evaluated the influence of the QCSE and impact ionisation and considered the relevance of these to developing a QD based optical modulator grown on silicon.

3.7 References

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Chapter 4

High-performance InAs/GaAs QD Lasers on GeSubstrates

This chapter describes the epitaxial growth techniques applied to III-V compound on-Ge substrates (III-V/Ge) material studies and further III-V/Ge QD device characterizations. The realization of semiconductor laser diodes on Si substrates would permit the creation of complex optoelectronic circuits, enabling chip-to-chip and system-to-system optical communications. Direct epitaxial growth of III-V semiconductor materials on Si or Ge substrates is one of the most promising candidates for the fabrication of electrically pumped light sources on a Si platform.

Incorporating photonic components into Si microelectronics has been the impetus behind the development of Si photonics for the last 30 years[3]. Although Si-based light generation and modulation technologies have been explored extensively[5], a Si-based laser has been considered the holy grail of Si photonics because (i) it is the most important active photonic device, (ii) the potential market for Si integrated circuits incorporating electrically pumped lasers is very large, and (iii) it is one of the most difficult challenges to realize among all the Si photonic components[4]. Si and Ge have an indirect band structure, which means radiative recombination events do not occur frequently and, accordingly, radiative recombination processes for emitters are insignificant compared to non-radiative recombination[4]. Direct bandgap III–V compounds have robust photonic properties that can be used for many photonics applications. Integrating III–V photonic components with Si

micro- electronics would thus provide the ideal solution for Si photonics.Although III-V/Si QD lasers by direct epitaxial growth have been demonstrated here in UCL, RT lasing has only been achieved under pulsed operation, due to dislocations generated at the GaAs/Si interface and propagating into the III-V active region[9]. To date, the most successful approach to the realization of III–V lasers on Si has been hybrid integration using wafer bonding, which has yielded devices capable of operating up to 65^{o}C. However, despite research activities stretching back over twenty years, the direct monolithic integration of III–V lasers on Si substrates continues to present huge implementation challenges[10].

To avoid the formation of threading dislocations, an alternative to direct growth of GaAs on Si is to use an intermediate epitaxial layer, which creates a near-GaAs lattice constant but has few defects.Because the Ge lattice constant is very closely lattice-matched (only 0.08% mismatch) to GaAs, Ge-coated Si layers (Ge/Si) have been widely used as an ideal 'virtual substrate' for subsequent GaAs growth[1]. Ge/Si based substrate has been a mutual technology for mass production. Therefore, Ge appears to be the best candidate of an intermediate buffer for GaAs growth.

Here, we describe the first quantum-dot laser to be realized on a Ge substrate. To fabricate the laser, a single-domain GaAs buffer layer was first grown on the Ge substrate using the Ga pre-layer technique. A long-wavelength InAs/GaAs quantum-dot structure was then fabricated on the high-quality GaAs buffer layer. Lasing at a wavelength of 1305nm with a threshold current density of 55.2A/cm^2 was observed under continuous-wave (cw) current drive at room temperature. The results suggest that long-wavelength InAs/GaAs quantum-dot lasers on Si substrates could be realized by epitaxial growth on Ge/Si substrates.

4.1 Surface Morphology

III–V lasers have not become well established on Ge substrates so far because of the formation of antiphase boundaries (APBs), which are planar defects and debilitate device performance. For conventional III–V quantum-well (QW) devices, any threading dislocation (TD) or APB propagating through the QWs will become a non-radiative recombination centre[11], leading to an increased threshold current density (J_{th}) for III-V QW lasers on

Geand Si substrates[10]. In the past decade, III–V QD—semiconductor nanosized crystal—lasers have been demonstrated with a significantly lower J_{th} than semiconductor QW lasers and offering temperature-insensitive operation above room temperature (RT)[13]. Furthermore, QD structures offer other unique advantages over conventional QWs for semiconductor lasers, including lower sensitivity to defects and the special capability of filtering the APBs and threading dislocations[15]. In the case of relatively high threading dislocation density in the active region, one threading dislocation in the active region can only 'kill' one or a few dots. It will not affect the majority of the quantum dots, so will not significantly degrade the performance of QD devices on Ge or Si substrates[17]. These novel attributes of QD technology are very promising for the development of III–V QD lasers on Ge substrates, and therefore on Ge/Si substrates. Recently, the growth ofInAs/GaAs QDs on a Ge substrate has been demonstrated[18]. However, the emission wavelength of InAs/GaAs QDs on Ge is only ~1.1 μm below room temperature, and there has been no report yet of the realization of lasers.

Although there could potentially be much fewerTDs generated by the misfit betweenGaAs and Ge, in comparison with GaAs and Si, the generation of APDs cansignificantly increase the surface roughness of the epitaxial layers, hindering large area uniformity. It should be mentioned that a flat surface is a prior condition for the formation of high quality QDs[14]. APDs due to polar crystal on non-polar crystal can be reduced by deliberately using mis-oriented Ge substrate [100] with 6^{o} off-cut towards [111] plane, as described in Chapter 2, which helps to ensure that the APDs are confined only close to the III-V/IV interfaces. Besides the substrate orientation, the initiation of GaAs with the typical procedure of using anAs or Gapre-layer would strongly affect the quality of the GaAs buffer layer, such as the surface roughness and defect density[16]. We have investigated both Ga and As pre-layer growth techniques. The surface morphologies of aGaAs buffer, and later, a Ga andAs pre-layer during the initial GaAs nucleation are shown in Figure 4.1. The most striking difference in Figure 4.1 is the absence of the large APD-related surface structures, and the surface roughness is thereby greatly improved, with a room-mean-squared (RMS)roughness less than 1 nanometer. Very importantly, this smooth surface is maintained for >1μm thick GaAs films, which indicates the formation of a single domain GaAs buffer layer on Ge substrate.

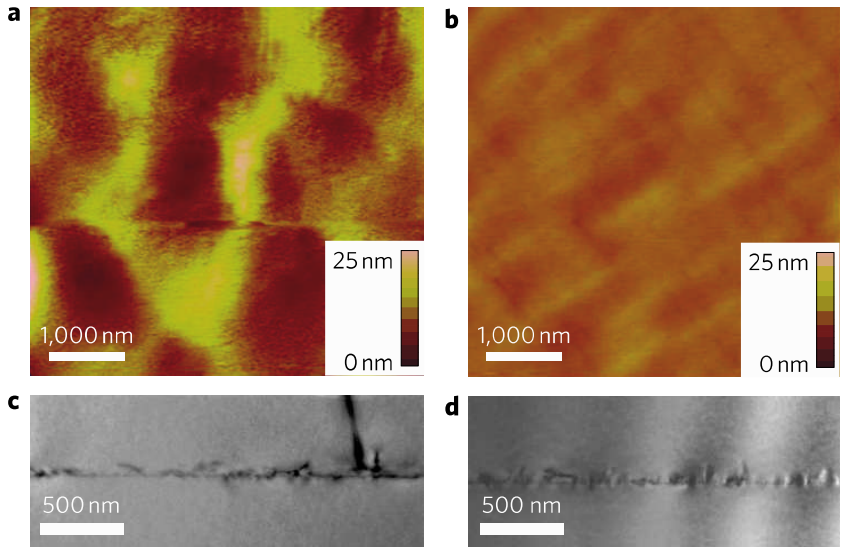

Figure 4.1: Structural properties of GaAs buffer layer on Ge substrate. The top are the AFM images (5 × 5 mm^2) of the surface morphology for 1.2 μm GaAs on Ge substrates with a) As pre-layer and b) Ga pre-layer growth techniques. The bottom are the TEM images of the interface between the GaAs buffer layer and the Ge substrate with c) As pre-layer and d) Ga pre-layer growth techniques.

Transmission electron microscopy (TEM) studies indicate that the defects are only observed within 150 nm of the GaAs/Ge interface for the sample using the Gaprelayer approach (Figure4.1d). The formation of defects at the GaAs/Ge interface is due to the relaxation of strain between the GaAs and Ge in the case of a thick GaAs layer. For the sample with an Asprelayer, APBs are generated at the GaAs/Ge interface and propagate into the GaAs buffer layer (Figure 4.1c).

4.2 Optimization of GaAs Nucleation Temperature

InAs/GaAsQD samples were fabricated on Ge substrates by UCL solid-source MBE. The schematic layer structure is illustrated in Figure 4.2.The Ge wafer is first treated with de-oxidation at 400^{o}C in the MBE chamber. The Ge substrate wasthen annealed at 640^{o}C to generate a predominantly doubleatomic-height step. After that, the Ge wafer was cooled down,following by depositing 30nm GaAs at three different temperatures of 350^{o}C, 380^{o}C and 400^{o}C with Ga pre-layer technique. During the Ga pre-layer process, the main shutter is first closed to cover the wafer, in order to prevent the diffusion of background As. The

Gasource is then deposited onto the Ge surface immediately, while the main shutter is open. Once the Ge substrate is completely covered by a monolayer (ML) of Ga atoms, the shutter of As source can be opened to form the first layer of GaAs. Therefore, the GaAs growth was nucleated with a 20-monolayer migration echancedepitaxy (MEE) step with this Ga pre-layer. Under the same conditions, 30nm of GaAs was grown subsequently at a slow growth rate of 0.1 ML/s, followed by 170nm higher temperature (500^{o}C) GaAs at a faster growth rate of 0.61 ML/s to assure the restraint of Ge-inter diffusion. Then, 800nm thick conventional high temperature (HT) GaAs at 580^{o}C was grown to create a high-quality single domain GaAs buffer with low defect density. The sample was further annealed at 700^{o}C to restructure the interface atomic bonding.

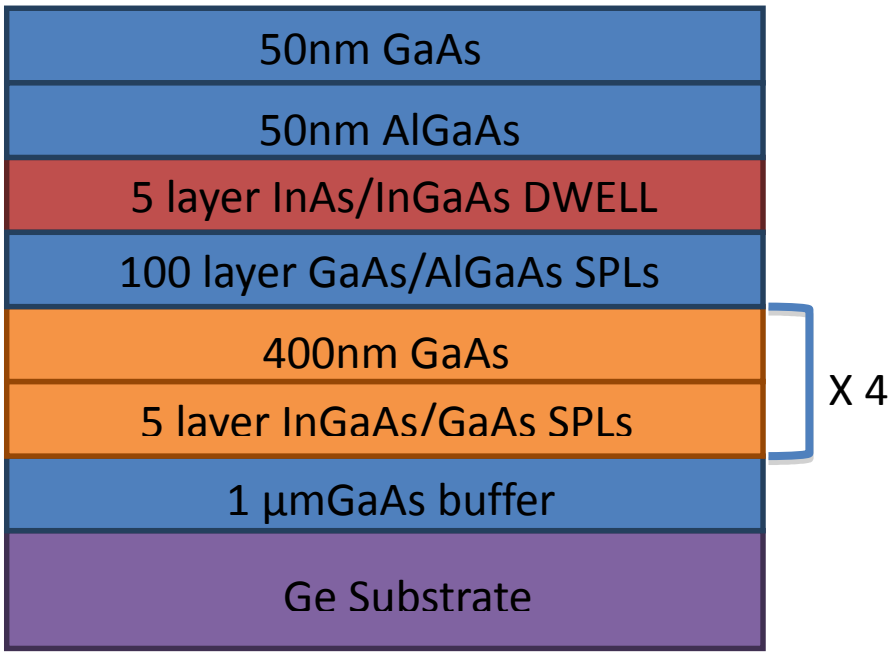

Figure 4.2: Cross-sectional schematic of InAs/InGaAs dot-in-a-well (DWELL) on Ge substrate.

There is a 1.5µm thick III-V buffer layer epitaxiallygrown on Ge substrate, followed by the structure of conventional InAs/GaAs QDs. Differing from conventional GaAs buffer layers, which requires a minimum thickness of 2 µm to achieve a flat surface, by using Ga pre-layer here, only 1µm GaAs buffer layer is deposited, followed by the multiple quantum well (MQW) dislocation filter structures.The dislocation filter is made up of 5 InGaAs quantum well layers separated by 10 nmthick of GaAs layers.

The structure is almost free of APDs and the dislocation density at the surface is estimated to be $8 \times 10^5\,cm^{-2}$ by incorporating anInGaAs/GaAsMQW dislocation filter within the buffer layer. Cross-sectional TEM studies in Figure 4.1 have also suggested that the defects generated at the GaAs/Ge interface are confined within 100nm of the interface.

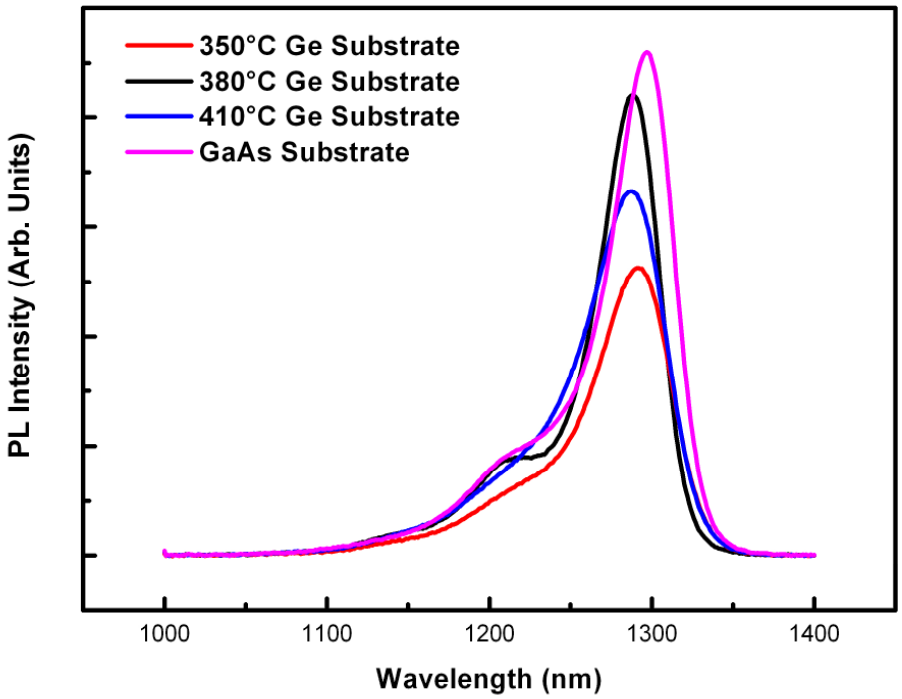

Figure 4.3: Room temperature PL spectra of InAs/GaAs QDs grown on Ge substrate with different growth temperatures for the initial GaAs nucleation layer. The room temperature PL spectrum of InAs/GaAs QDs grown on GaAs substrate is also shown as a reference.

Apart from theGa pre-layer technique, which we use to grow single domain GaAs on Ge substrates,the different substrate temperaturesfor the GaAs nucleation layer can strongly affectthe optical properties of 1300-nm InAs/GaAs QDs grown on Ge substrates. By comparing the PL spectrum of samples with the initial GaAs nucleation layers at 350°C, 380°C and 410°C, the PL intensity and linewidth plots indicate that 380°C appears to be the optimum growth temperature for the initial GaAs nucleation layers, as shown in Figure 4.3. With the optimum GaAsnucleation temperature at 380°C, the PL intensity of InAs/GaAs close to the level of QDs grown on GaAs substrate is achieved. It should be mentioned that the reference InAs/GaAs QDs were grown under optimized conditions and represent very

high optical quality as the QD laser diode based on identical growth parameters gives an extremely low $J_{th}$and high output power at RT[21].

Of considerable significance is that the PL intensity of the ground-state transition of InAs/GaAs QDs grown on the Ge substrate is strongly dependent on the growth temperature of the initial GaAs nucleation layer. The strongest PL intensity for InAs/GaAs QDs on a Ge substrate is obtained from the sample grown with a GaAs nucleation temperature of 380^{o}C, and is almost identical to that of reference QDs grown on GaAs substrate.

To further understand the effectiveness of the nucleation temperature changes the quality of QD growth, the AFM images of surface QDs are studied in section 4.3.

4.3 AFM Studies of Surface InAs/GaAs QDs

In order to examine the growth quality of buffer structures, AFM images of surface grown InAs QDs are studied here to further verify the results. The surface InAs QD layer is grown on a 2nm thick InGaAs layer. The QDs were grown at 510 ^{o}C with a deposition rate of 0.093ML/s and a total amount of InAs of 2.79ML. Figure 4.4 shows an AFM image for an uncapped InAs QDsample grown on a Ge substrate with aGaAs nucleation temperature of 380^{o}C [21], in which the growth was terminated immediately after the dot deposition. Atomic force Microscope (AFM) measurements were performed for all samples with a Nanoscope Dimension 3100 AFM system in ambient conditions using a noncontact mode.The root-mean-square surface roughness before the dot depositionat different GaAs nucleation temperature was similar (< 1 nm). A dot density of $4.3\times10^{10}cm^{-2}$ is estimated from this image. Although any In-Ga intermixing occurring after the dot growth may modify the dot properties, it is believed that this figure gives a reasonable estimation of the dot density and size in the corresponding optical sample. Here, a low growth rate is normally preferred to form large dots for long-wavelength emission at 1300 nm. On the other hand, the dot density will also be reduced to a lower level, which can degrade the intensity of PL. Therefore, a moderate growth rate of 0.093ML/s is used to achieve a balance between dot density and emission wavelength.

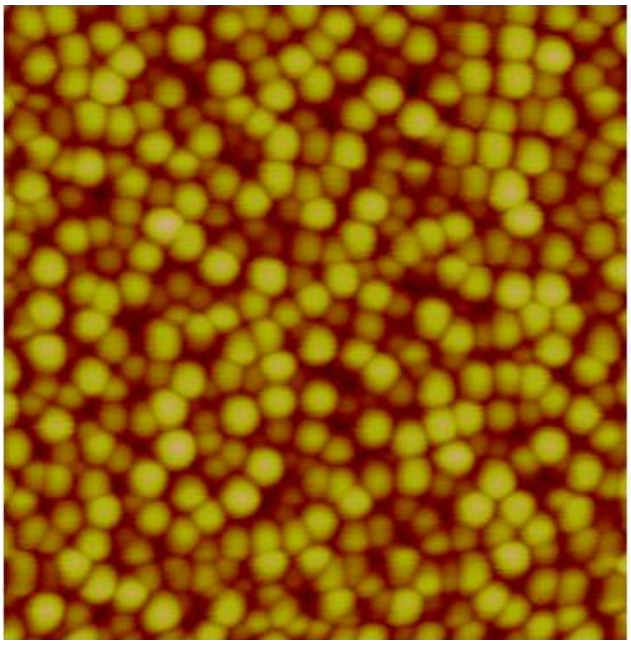

Figure 4.4: 1×1μm^{2}AFM image of uncapped InAs QDs grown on Ge substrate with aGaAs nucleation temperature of 380^{o}C.

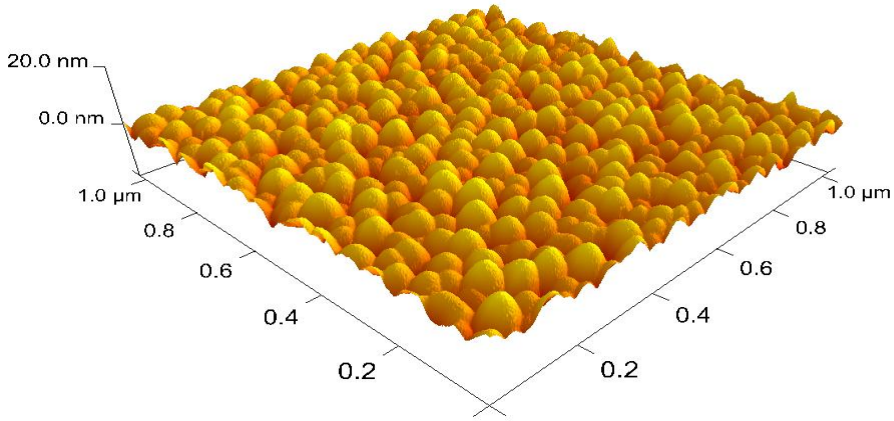

Figure 4.5: 1×1μm^{2}3D AFM image of InAs QDs on Ge substrateaGaAs nucleation temperature of 380^{o}C.

The AFM results shown in Figures 4.4 and 4.5 indicate that InAs QDs randomly distribute on the surface, as on GaAs substrates[22]. The 3D AFM image in Figure 4.5 shows the formation of nearly uniform QDs with no undulation in the wetting layer. The height of QDs is in the range between 4nm and 12 nm. This morphology of InAs QDs in Figure 4.4 is

significantly different from that of InAs/GaAs QDs grown on a Ge-on-insulator-on-Si substrate by metal organic chemical vapour deposition, in which APBs were observed and the InAs QDs were lined with a preferential orientation along the [1$\bar{1}$0] direction with bimodal size distribution[23].

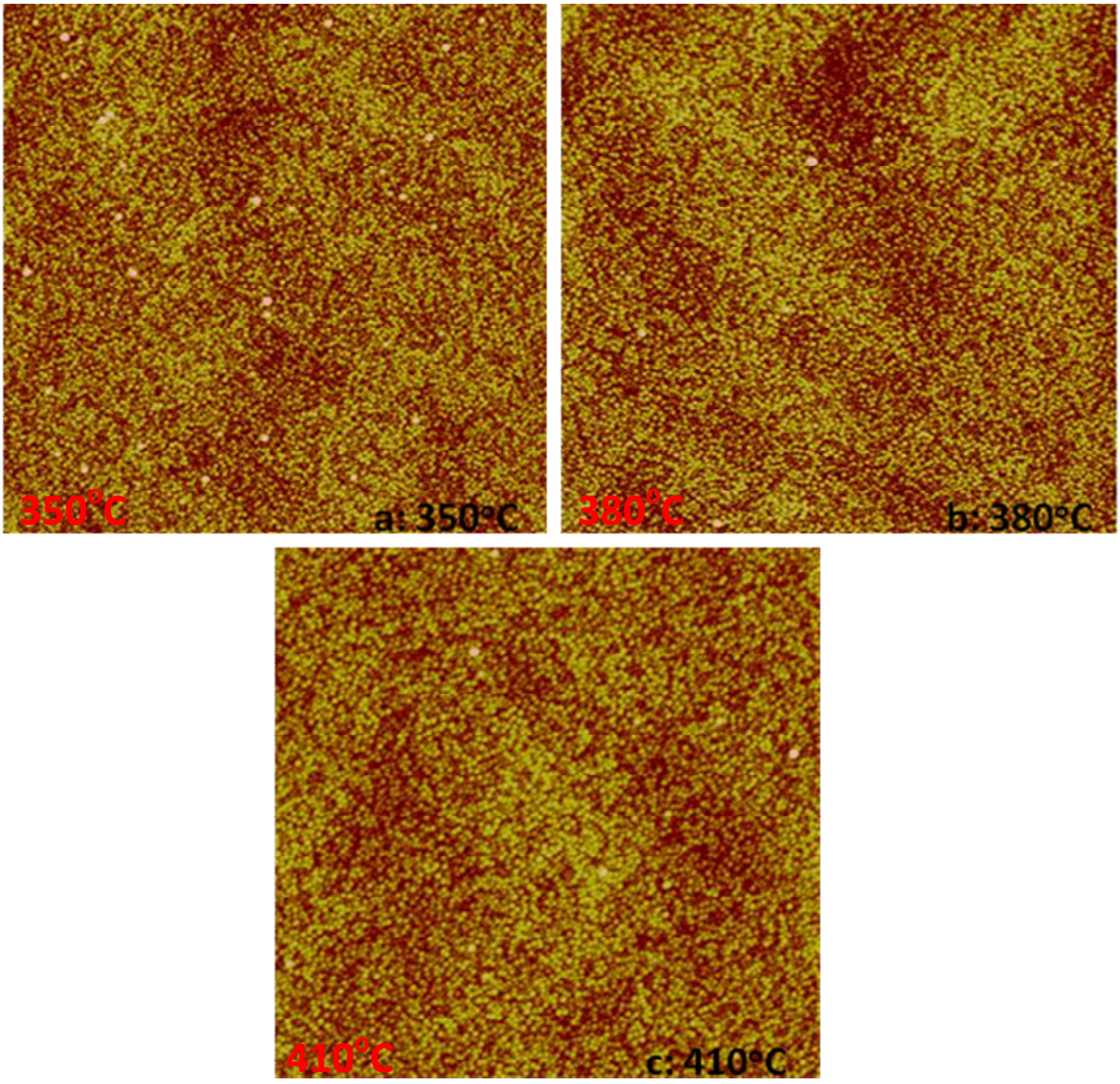

Figure 4.6: 9×9μm^2 AFM images of surface InAs QDs with different GaAs nucleation temperature a) 350°C, b) 380°C and c) 410°C.

To further study the effectiveness and importance of these initial procedures for growing GaAs on Ge substrate, large-scale AFM images of uncapped QDs based on three different nucleation temperatures, have been compared in Figure 4.6.In principle, the

defects at the GaAs/Ge interface would either propagate into the active layers or result in undulation of the top grown surface. Therefore, this would lead to a high defect-dot density after the top QDs growth. Defect-dot densities of 3.1×10^{7}, 6.2×10^{6}, and 9.9×10^{6} cm^{-2} were obtained for the samples with the initial GaAs layer nucleated at 350, 380, and 410 ^{o}C, respectively, in Figure 4.6.We can conclude that the growth quality of QDs is highly dependent on the initial growth procedure at the Ge/GaAs interface.

4.4 Cross-sectional Transmission Electron Microscopy

Transmission electron microscopy (TEM) measurements were performed to compare the structural properties of GaAs/Ge interfaces with different GaAs nucleation temperatures.

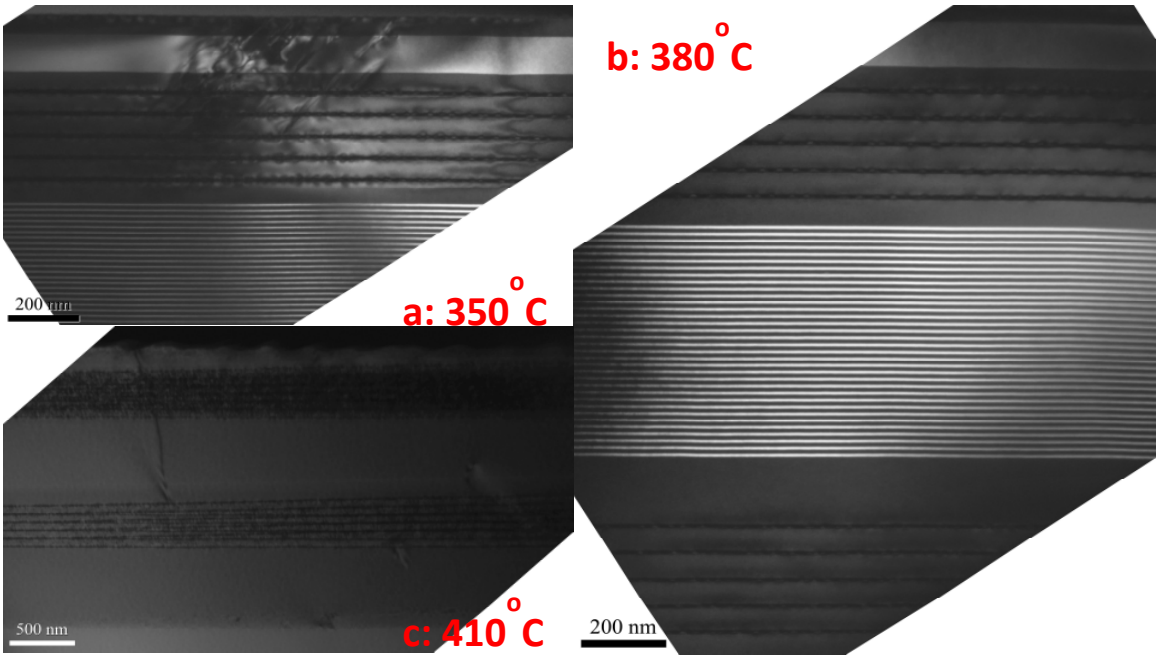

Figure 4.7: Cross-sectional TEM images of epitaxial structures at different nucleation temperature a) 350^{o}C, b) 380^{o}C and c)410^{o}C.

Figure 4.7 shows the cross-sectional TEM images of three identical sample structures with three different GaAsnucleation temperatures. The defects nucleate at the GaAs/Ge interface for all three samples due to the small lattice mismatch between GaAs and Ge for a thicker epitaxial layer.

It is reported that a transition temperature of 600^{o}C is required to form double atomic-height steps at the single-stepped Ge surface[2]. In our case, all three samples are deposited with in-situ annealing at 640^{o}C. Mostdefectsare confined within 50 nm of GaAs/Ge interface while some propagate into the III-V buffer layers. In both Figure 4.7a and c, which are grown at lower and higher temperature, large numbers of TDs propagating into the active layers have been observed. However, TDsare not observed in images of the sample with an initial nucleation temperature of 380 ^{o}C in Figure 4.7b.

4.5 Temperature and Power Dependent Photoluminescence

In order to determine their adequacy for optoelectronic applications, the optical properties of the grown InAs/GaAs QD layers on Ge substrates have been investigated by temperature dependent PL measurements as shown in Figure 4.8.

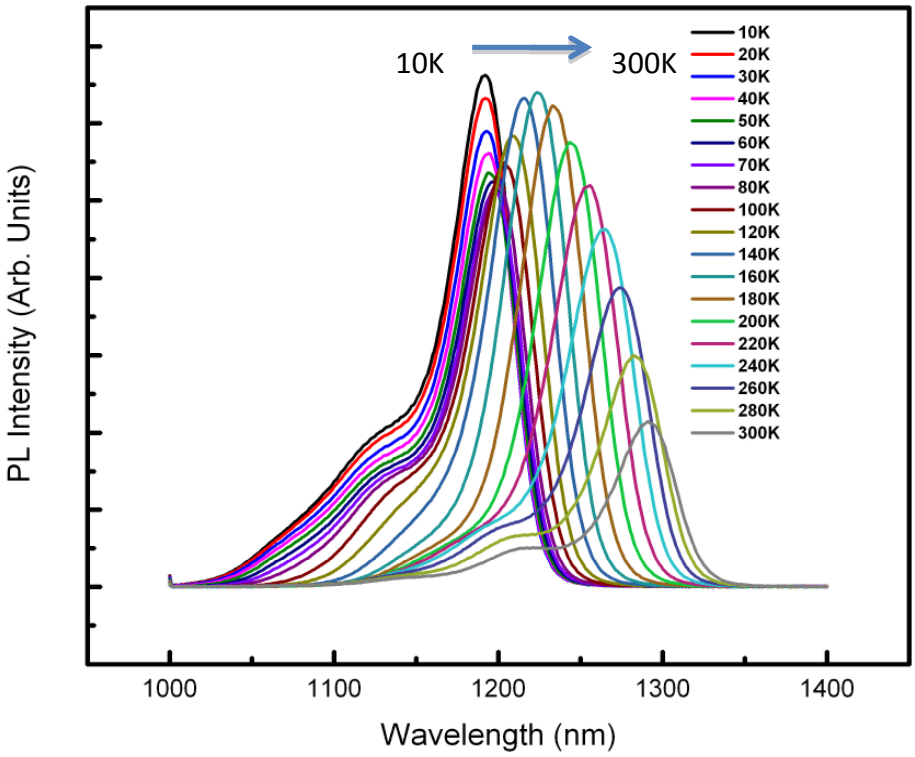

Figure 4.8: Temperature-dependent PL spectra ranging from 10K to 300K.

All samples were mounted on a flat copper plate within the cryostat under accurate temperature control. A solid-state diode pumped laser, emitting at 532nm, was used as an

excitation power. The emitted radiation from the material is collected by the Newport Cornerstone 1/4m monochromator and detected by a TE-cooled Ge detector. A fixed laser power of 5 mW is here used for temperature-dependent PL measurements for all samples. The low excitation power is used to prevent heat accumulation in the sample, which can lead to a red shift in the emission wavelength. The temperature-dependent PL spectra are shown in Figure 4.8. The PL intensity drops gradually from 10K to 80K, and then starts rising again before the PL intensity repeats the decrement from 160K to 300K. The sudden rise of peak PL intensity between 10 and 80 K is believed to be caused by the thermal excitation from smaller QDs to the larger ones.

4.5.1 Arrhenius Plot of the PL Intensity

To further investigate the mechanisms of the temperature dependence of GaAs nucleation, we studied the integrated PL intensity (IPLI) in the temperature range from 10-300K. With a low laser power excitation, only ground-state emission was present in the PL. Figure 4.9 shows the Arrhenius plot of the IPLI for three different growth temperatures of the GaAs nucleation layer. The variation of IPLI data with temperature can be described by the generic empirical relationship:

$$( ) = \frac{\blacksquare}{1 + \ _{1}\ ^{-}\!\!-} \quad (1)$$

where E is the thermal activation energies (TAE) for loss mechanisms active at certain temperature ranges, k is the Boltzman constant, T is the temperature, and I_0 and C_1 are fitting constants[24].

In a physical model, these constants would take into account the recombination rates and the geometric dimensions of the dots. The IPLI of all three samples remain constant from 10K upto 77K, and then decreases until RT. Although the IPLI starts dropping dramatically above 77K, the IPLI still remainspersistent at a high level, which is attributed to the increase in oscillator strength due to additional lateral confinement in QDs compared to conventional quantum wells.The slope of the lines at high temperatures yields thermal activation energies of ~222meV, ~242meV and ~236meV, corresponding to the growth temperatures at 350^{o}C, 380^{o}C and 410^{o}C, respectively. The thermal activation energies are similar to the energy difference between the QDs ground state (GS) and InGaAs conduction

band edge[24], which verify that there are no significant band structure variations caused by changing the nucleation temperature. It is well established that the reduction in IPLI is attributed to the thermal escape of carriers from QD ground states into the InGaAs QWs followed by non-radiative recombination in the barriers. Therefore, the IPLI differences among three samples shown in Figure 4.9 could be understood in terms of the different density of defects generated at GaAs/Ge interface and propagating into the III-V active region. This is further confirmed by etch-pit density (EPD) measurements. The etchant used for the EPD delineation is a mixture of H_3PO_4, H_2O_2, and H_2O (in a 1:1:3 ratio). Defect densities of 1.7×10^7, 8.0×10^5, and 3.7×10^6 cm^{-2} were obtained for the samples with the initial GaAs layer nucleated at 350, 380, and 410 ^oC, respectively.

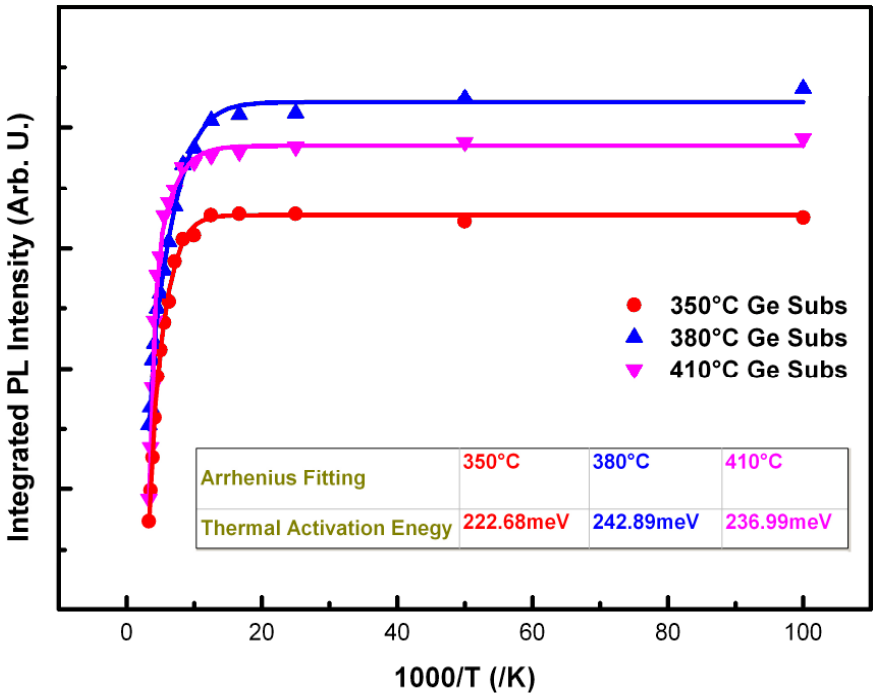

Figure 4.9: Arrhenius plots of the IPLI of InAs QD samples on Ge with three different nucleation temperaturesof 350^{o}C, 380^{o}C and 410^{o}C.

QD formation is extremely sensitive to the surface roughness and defect density of the buffer layer.Therefore, the structural properties of buffer structures directly determine the emission strength of QDs. In general, relatively low temperature of 350^{o}C generates significantly more defected dots than the other two due to its poor material quality and high

TD density at low temperature nucleation. At 380°C, the higher temperature has provided atoms with much higher mobility to move around in order to eliminate surface defects. But excess thermal energy can also induce strong atomic movement, therefore, damage the sample surface, which explains the PL degradation at 410°C. This is confirmed by the EPD and AFM measurements discussed above.

Temperature-dependentPL spectroscopy of these three samples permits a comparison of both the bandgap and the dot inhomogeneity of the structures. Spectra recorded from three different samples are shown, as measured at low temperature (10K) with a relatively high excitation power of 100mW.

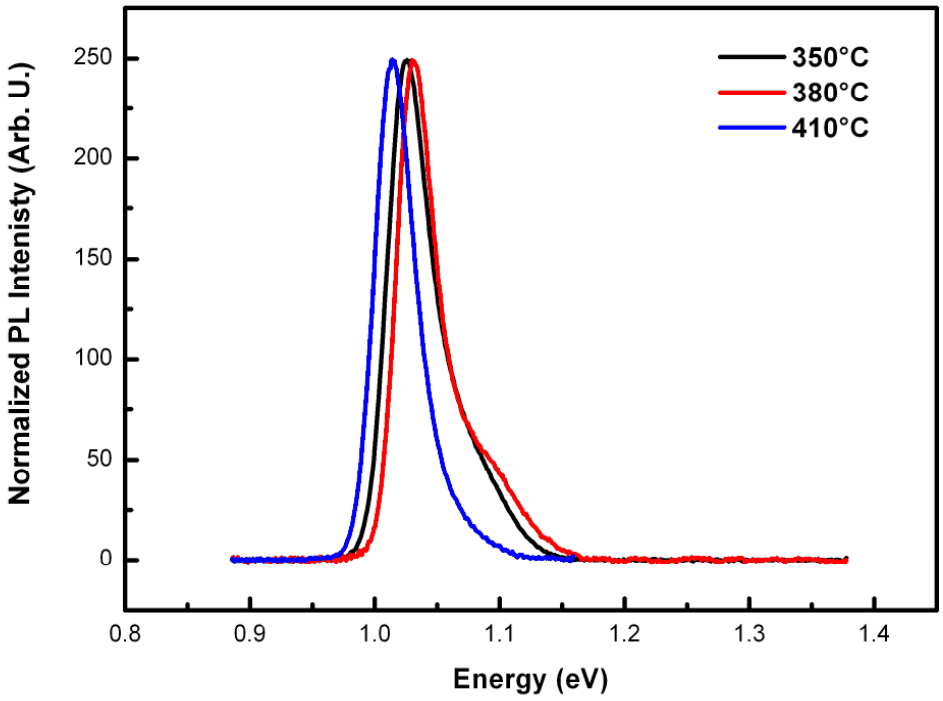

Figure 4.10: Normalized 10K PL spectrum of InAs QDs samples grown with three different nucleation temperatures at 350°C, 380°C and 410°C.

From Figure 4.10, the PL of sample grown at 350°C, centred at 1.035eV, is red-shifted by 5meV compared to the sample with 380°C nucleation temperature, which is centred at 1.04eV. Thesample grown at 410°C corresponds to the lowest energy at 1.02eV, which is red-shifted by 20meV. As the PL intensity is normalised here, the quality of QD emission can be determined by the observation of excited-state emission at 10K, where the thermal

escape of carriers is weak. Therefore, under high power excitation, the excited-state emission arises in the condition of low defect density. In this case, sample with a nucleation temperature of 380°C appears to have the strongest contribution from excited-state emission.

4.5.2 FWHM Plots of the Temperature Dependent PL

It can be observed from Figure 4.11 that the full-width-half-maximum(FWHM) of the PL spectrum varies between 33 to 37meV for sample grown at 380°C in the whole temperature range from 10K to 300K. The sample has the least variation of 12% and narrowestroom-temperature linewidthamong all samples.

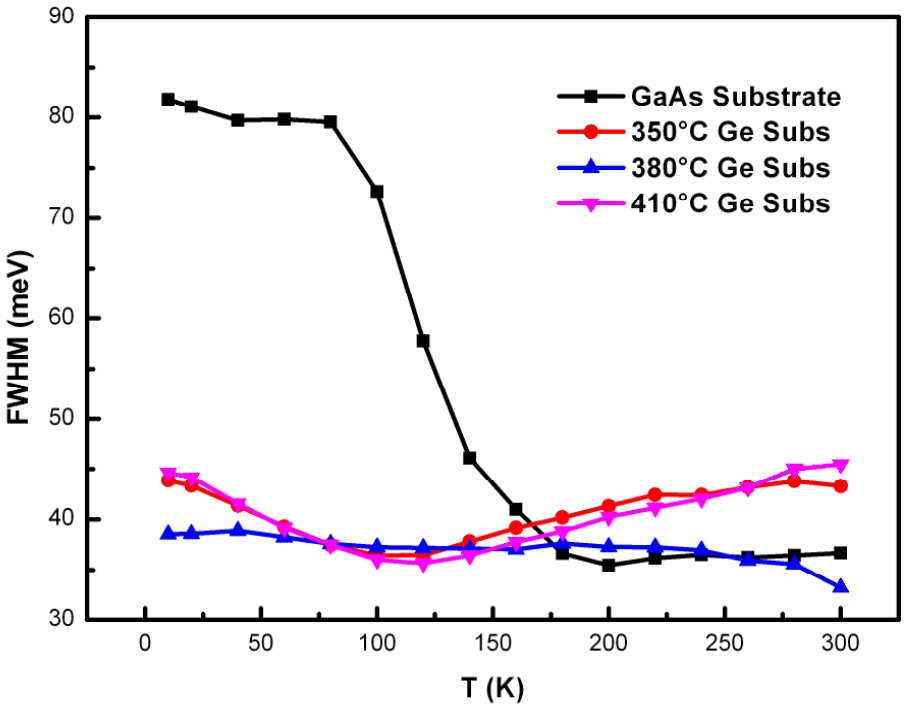

Figure 4.11: PL linewidth (FWHM) versus temperature plot for InAs QD samples on Ge with three different nucleation temperatures at 350°C, 380°C and 410°C, including an additional reference sample grown on a GaAs substrate.

In comparison, samples grown at 350°C and 410°C have larger variations of 20% and 25%. The reference sample grown on GaAs substrate has the largest FWHM variation for

temperature-dependent PL, because the appearance of the emission from small QDs at low temperatures (below 200K) broadens the FWHM of the spectrum. At room temperature, a relatively narrow linewidth of ~36 meV is still observed for the reference sample on the GaAs substrate, where sample grown at 380 ^{o}C shows the narrowest linewidth of ~33 meV. Both samples grown at 350 ^{o}C and 410 ^{o}C have broader linewidth at ~43 meV and ~45 meV.

In principle, the FWHM of the reference sample on the GaAs substrate is expected to be small at 10K. However, a broad linewidth of 82.3meV is observed here in Figure 4.11, which can be explained as the bimodal size distribution of QDs and the emission from excited state in this reference sample. Although the FWHMs are hard to be compared at 10K due to small QD emission and strong excited-state emission, the RT linewidths at 300K still show the relatively narrow FWHMshave been achieved by both the GaAs reference sample and the sample on Ge at the nucleation temperature of 380^{o}C.

4.5.3 Power Dependent PL

An example of the development of QD emission with increasing injection power is demonstrated in Figure 4.12 at 10K. For low excitation power the PL spectra exhibit a strong ground state emission. As the injected optical power is increased, the ground state intensity initially increases and then saturates. The first excited state transition is observed as a high-energy shoulder but will develop into the dominant emission at high excitation power. In Figure 4.12, the excitation power was only increased upto 70mW, as there is significant red shift occurring above this power due to heat generation within the sample. But the rise of first excited state transition can still be observed here proportional to the rising optical pumping power. The ground state emissionwill start to saturate above 100mW due to limited electron-hole recombination rate,and the excessive power will transit to high energy levels, leading to the first excited state emission at1121 nm.

The occurrence of the first excited state transition is caused by the strong carrier confinement at 10K, where carriers have filled discrete ground states within InAs QDs. With increasing excitation power, the carriers will accumulate at the first excited states, as the ground states remain filled. The excessive electrons and holes will recombine at the first excited states, generating the first excited state emission. The quick rise of excited state

emission indicates a good three-dimensional carrier confinement within the InAs QDs, as the escape rate of carriers is slower than the carrier injection rate. If the defect density is high, the carrier leak and escape from QD excited states towards defects would occur.

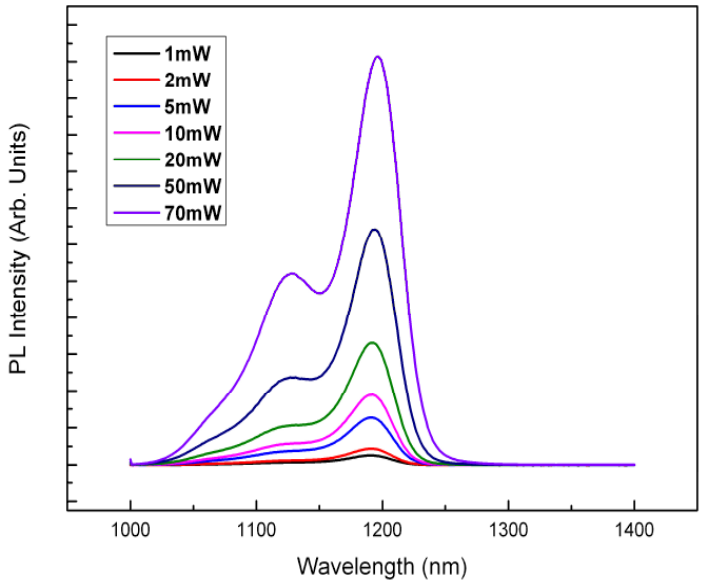

Figure 4.12: Power dependent PL spectra with excitation power from 1mW to 70mW at a measurement temperature of 10K.

4.6 Laser Characteristics

A five-layer InAs/InGaAs dot-in-a-well (DWELL) laser structure was fabricated on a single-domain GaAs buffer layer. The device structure of the QD laser on a Gesubstrate is shown in Figure 4.13a.The top-view microscope image of this device is shown in Figure 4.13b and c.

The laser was grown on a p^+-doped Ge substrate and consisted of the following layer sequence. Beside the buffer growth as described in section 4.1, a 1.5-μm p^+-doped GaAs buffer layer and a 1.5-μm $Al_{0.4}Ga_{0.6}As$ p-doped cladding layer were deposited first, followed by a 55-nm $Al_{0.2}Ga_{0.8}As$ guiding layer and a 70-nm GaAs barrier layer. Standard 5-layer 1300-nm InAs/InGaAs DWELL lasers were grown subsequently. Following that, a 70-nm GaAs barrier layer, a 55-nm $Al_{0.2}Ga_{0.8}As$ guiding layer, a 1.5-μm $Al_{0.4}Ga_{0.6}As$ n-doped cladding, and

a 300-nm n^+-doped GaAs contact layer were grown.The GaAs/AlGaAs cladding heterostructures provide electrical and optical confinement to the InAs/GaAs DWELL. The active region quantum dot layers, the GaAs layers and AlGaAs layers were grown at510, 580 and 600^oC, respectively. P and N type doping were accomplished with Be and Si, respectively.It should be mentioned that the InAs/GaAs QDs were grown under optimized conditions and represent very high optical quality as the QD laser diode based on identical growth parameters gives an extremely low $J_{th}$and high output power at RT[21].

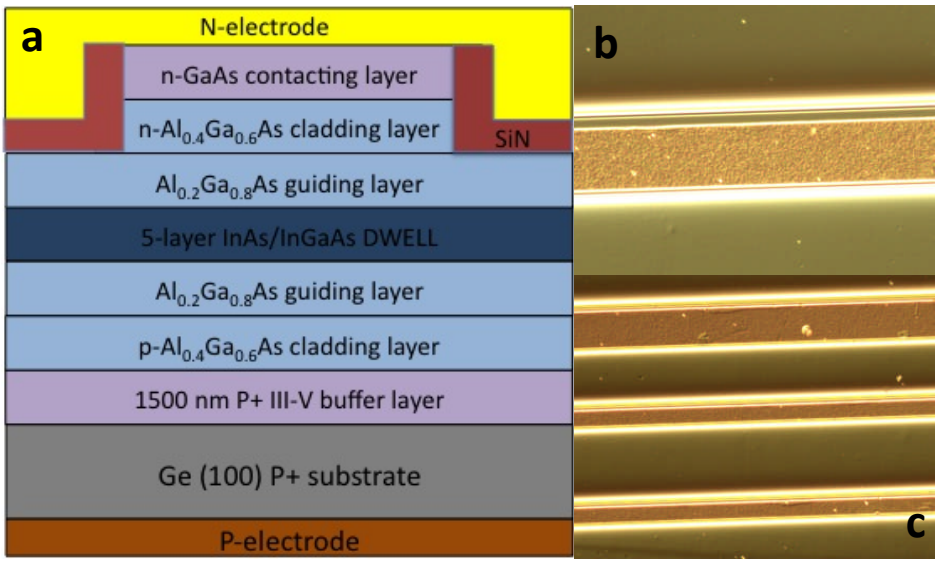

Figure 4.13: InAs/GaAs QD laser diode on Ge substrate. a) Cross-sectional schematics of the laser structure. b,c) The top-view microscope images of the device.

Broad-area laser device were formed with a shallow ridge etch (etch stops above the active layer with a depth of 1.8 μm and a width of 50 μm) after deposition of and Al contact layer on the bottom of the wafer for p-contact on theGe substrate. Wet chemical etching was terminated when the upper n-doped GaAs and n-doped AlGaAs layersabove the QD active region were removed to a depth of 1.8μm. A 500-nm-thick layer of SiN_x was deposited on the sample surface and contact windows opened on the ridge top, followed by deposition of the In/Ge/Au contact layer. Similar device processing procedures were used for GaAs-based QD devices apart from Au/Zn/Aubeing used as the top p-contact layer.

Broad-area devices with cavities of width 50 μm and 5 mm length were fabricated with as-cleaved facets. Figure 4.14a shows a series of room-temperature spontaneous emission and lasing spectra for a QD laser diode operating below and above threshold. The

laser diode was driven in continuous-wave (CW) condition.

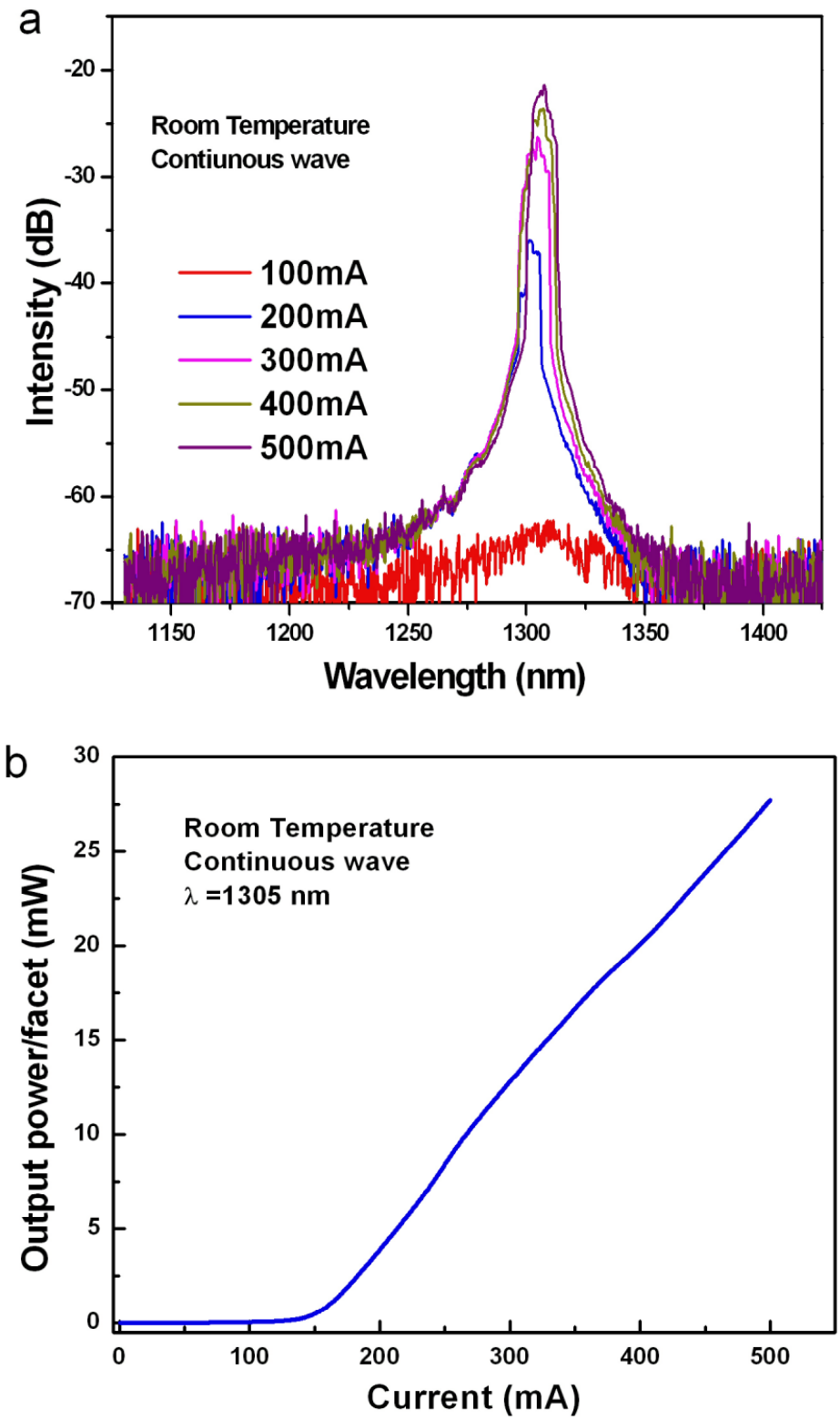

Figure 4.14: Room-temperature emission spectra and light ouput characteristics. a) Emission spectra of 5-layer Ge-based InAs/GaAs quantum dot laser for different drive currents below and above threshold. b)Light output against current for Ge-based InAs/GaAs QD laser.

Spontaneous emission can be observed at a peak wavelength of approximately 1306 nm with FWHM of 35 meV at a current of 100 mA.Lasing emission with peak wavelength of 1305 nm can be observed at a current of 200 mA, as shown Figure 4.14a. On increasing the injection current, the multimode lasing spectrum appears. Figure 4.14b shows the device light output power against current (L-I) characteristics under CW operation at room temperature.

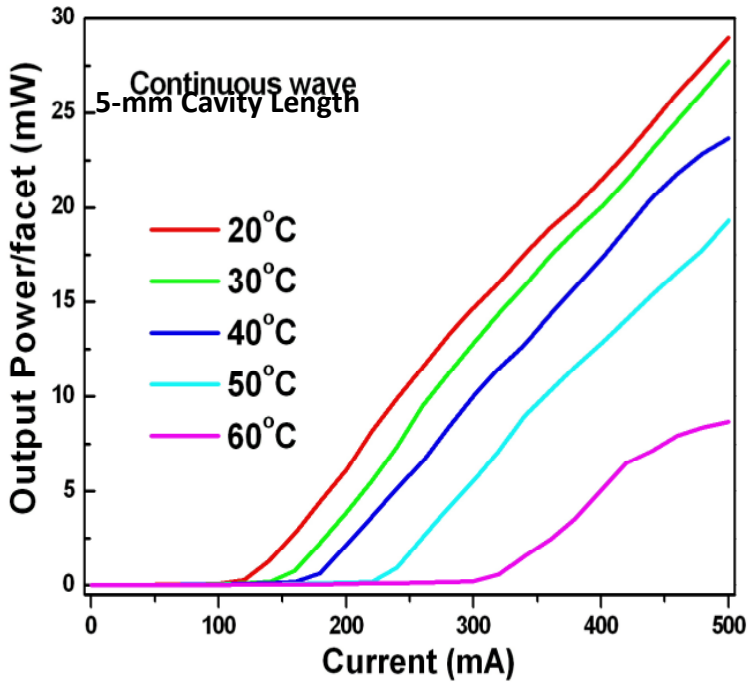

Figure 4.15: Temperature-dependent light output power characteristics. Light output against current for various substrate temperatures.

The measured output power from one facet is close to 28 mW for an injection current of 500 mA, with no evidence of power saturation up to this current. The lasing threshold is 138 mA. The threshold current density (J_{th}) is 55.2 A/cm^2, which corresponds to about 11 A/cm^2 for each of the five QD laser layers. This extremely low J_{th} is comparable to the best-reported values for GaAs-based multilayer InAs QD lasers. For example, the record value of RT CW J_{th} for GaAs-based QD lasers with as-cleaved facets is 32.5 A/cm^2 for both 3-QD-layer

ridge-waveguide lasers[21]. The threshold current densities of InAs/GaAs QD laser diodes are very sensitive to the defects within the active region. The extremely low threshold current density obtained for the Ge-based InAs/GaAs QD laser here clearly indicates that the defects generated at the GaAs/Ge interface and within the III-V buffer layer are very low, and hence that the quality of the GaAs buffer layer grown on the Ge substrate is very high.

Figure 4.15 shows the device CW output power per facet for various substrate temperatures, ranging from 20 to 60 ^{o}C. The laser has a 60 ^{o}C maximum lasing temperature with a characteristic temperature of about 40 K.In addition, the temperature sensitivity of this device is similar to those InAs QD laser devices reported on GaAs substrate.

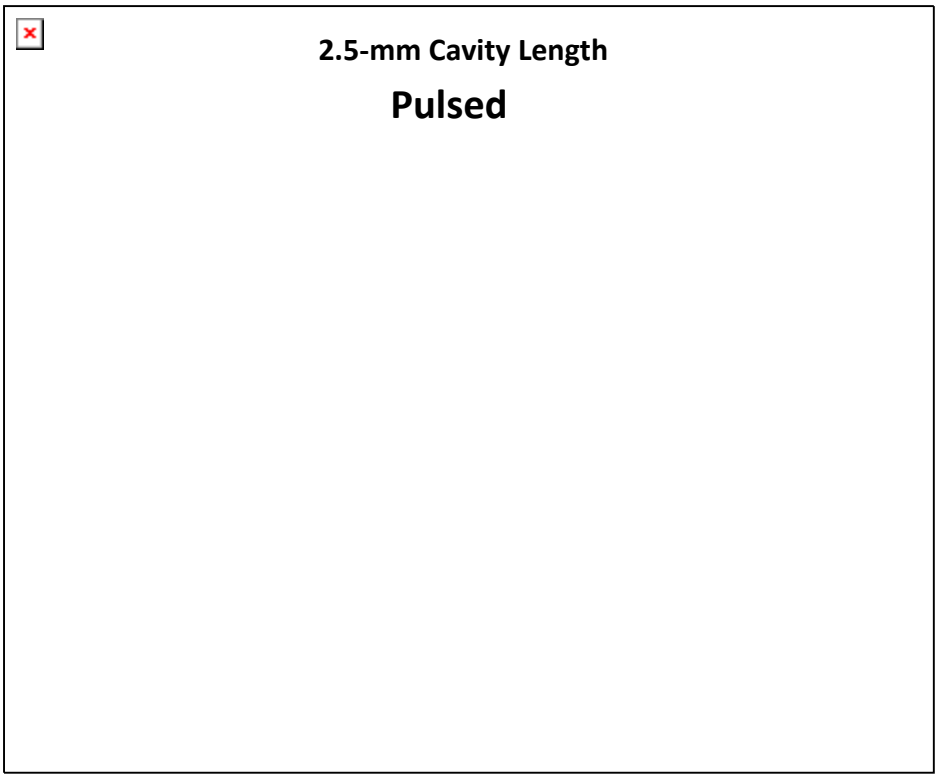

Figure 4.16: Light output against current characteristic for InAs/GaAs quantum-dot laser grown on Ge substrate for operating temperatures between 20 and 100 ^{o}C. The inset shows the laser optical spectrum above threshold at RT.

Note that techniques for fabricating low-defect Ge buffer layers on Si substrates have been systematically developed and high-quality Ge/Si wafers are commercially available. A next step towards developing long-wavelength InAs/GaAs QD lasers on Si substrates could be achieved by growing the laser structure on Ge/Si substrates. Here, it should be

mentioned that although an epitaxially grown Ge/Si laser operating at room temperature has recently been demonstrated by using tensile strain and n-type doping, it was pumped optically[18].

Devices with a shorter cavity length of 2.5 mm were further characterised under pulsed coditionswithout any mounting and bonding. Laser characteristics were measured in pulsed mode using a pulse width of 0.1 μs and duty cycle of 0.01%. The inset in Figure 4.16 shows the laser optical spectrum above threshold at RT, in which lasing at 1.306 μm is observed. The main part of Figure 4.16 shows the output power against current at various temperatures. A RT J_{th} of ~106 A/cm^2 is obtained, with lasing up to 100 ^{o}C and characteristic temperature, T_0 of 47 K between 20 and 100 ^{o}C, which is comparable to the performance of 1.3-μm InAs/GaAs QD lasers grown on GaAs substrates[27].

4.7 References

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Chapter 5

Design and Modelling of Ridge-waveguide Lasers

This chapter describes modelling techniques and presents simulation results for the design of ridge waveguides lasers and possible integrations. In section 5.1 and 5.2, guided-wave theory is firstly introduced with the propagation and confinement of light in the waveguides. Subsequently, in section 5.3, the transverse modes and propagation within one-dimensional planar waveguide is discussed. To compare, the transverse mode operations of ridge waveguides are studied and simulated in section 5.4.

A critical issue of the monolithic integration of the edge-emitting laser and guided-wave devices is the optimization of the optical coupling between both devices involving etched facet quality and waveguide dimension in a groove-coupling scheme. However, the planar edge-emitting laser beam is usually far from a Gaussian shape. Therefore, a ridge waveguide with optimized dimension is definitely required here to achieve an efficient coupling between the laser and guided-wave devices.

5.1 Waveguide and Light Confinement

The optical waveguide is originated from the realisation of the preference of light: light loves to travel in a medium with high refractive index. This discovery ensures the possibility of optical confinement within a refractive-index mismatched waveguiding system.

The schematic of the simplest three-slab waveguide analysis is shown in Figure 5.1. This waveguide consists of a high-refractive-index medium surrounded by the other two identical cladding layers with lower refractive index. If the cladding layer is sufficiently thick to overcome the evanescent field [1] associated with the modes, light can be confined mainly in the core layer as shown in the light intensity distribution in Figure5.1.

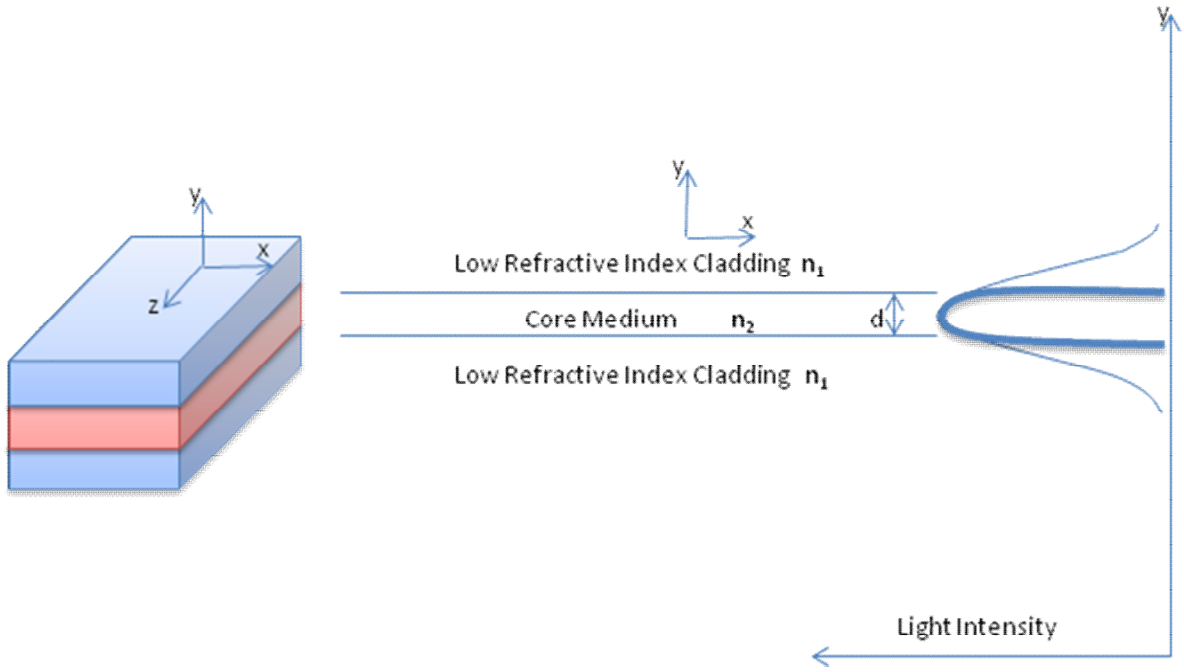
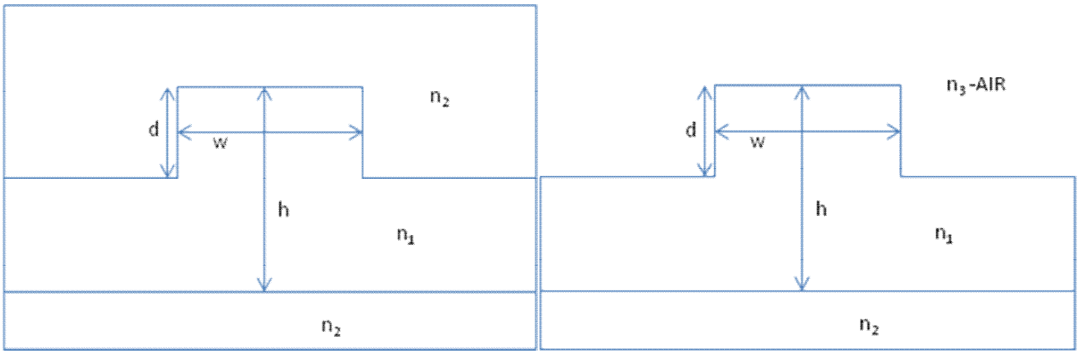


Figure 5.1: Symmetric three-layer slab waveguide with $n_2 > n_1$.

The slab waveguide has been extensively studied in the last century. The principles of the propagation of electromagnetic (EM) wave indicate that the waveguide supports two sets of field modes: transverse electrical (TE) and transverse magnetic (TM) modes[1], which are distinguished on the basis of their polarisations. The TE mode has the electric field polarised along the x axis, and the TM mode has the magnetic field polarised along the x axis.

In the case of the three-layer planar waveguide in Figure5.1, the mode confinement in the y direction is mainly due to the refractive index steps between the interfaces of core and claddings. But only one-dimensional confinement is not sufficient for practical applications, the most common being the so called rib or ridge waveguide by etching a two dimensional waveguide. The cross-section of a ridge waveguide is shown in Figure 5.2, where the

schematic in Figure 5.2a is a symmetric waveguide with the same upper and bottom claddings. In contrast, the schematic in Figure 5.2b is an asymmetric waveguide with a different upper cladding: air.



a: Symmetric ridge waveguide b: Asymmetric ridge waveguide

Figure 5.2: Geometries of symmetric and asymmetric ridge waveguide.

5.2 Basics of Electromagnetic Waves

The study of light is a study of electromagnetic waves. Therefore, to fully understand the behaviour of the optical waveguide it is necessary to use electromagnetic theory. According to the *Fresnel Formulae*, the optical behaviour at the interface of claddings and core is defined to be partial reflection and partial transmission[1]. For example, the reflected wave will have complex amplitude $E_r$at the interface, related to the complex amplitude E_i of the incident wave by:

$$E_r = rE_i$$

where r is a complex reflection coefficient. The reflection coefficient is a function of both the angle of incidence and the polarisation of light. Hence, the polarisation with respect to the interface has to be defined first.

The electric and magnetic fields of an electromagnetic wave are always orthogonal to each other, and both orthogonal to the direction of wave propagation. Hence propagating electromagnetic waves are also referred to as transverse electromagnetic waves, or TEM waves. The transverse electric (TE) condition is defined as the condition when the electric fields of the light beam are perpendicular to the plane of incidence shown in Figure

5.3.Correspondingly, the transverse magnetic condition is defined as the condition when the magnetic fields are perpendicular to the plane of incidence.

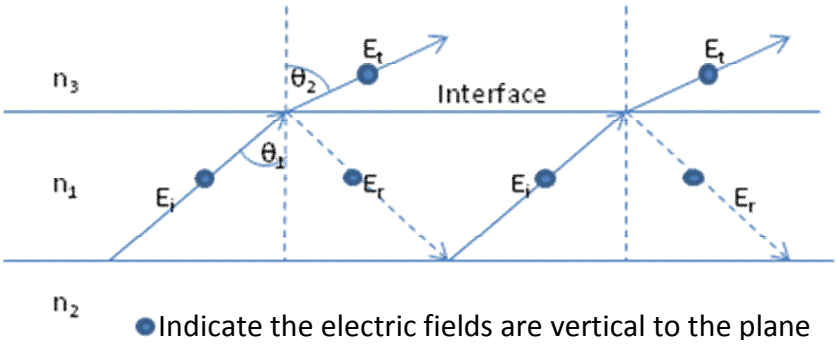


Figure 5.3: Light rays refracted and reflected at the interface of two media

The Fresnel formulae[2] describe the reflection coefficients with respect to polarisation r_{TE} and r_{TM} as follows:

$$r_{TE} = \frac{n_1 \cos\theta_1 - n_2 \cos\theta_2}{n_1 \cos\theta_1 + n_2 \cos\theta_2}$$

$$r_{TM} = \frac{n_2 \cos\theta_1 - n_1 \cos\theta_2}{n_2 \cos\theta_1 + n_1 \cos\theta_2}$$

Snell's Law is given by:

$$n_1 \sin\theta_1 = n_2 \sin\theta_2$$

Applying Snell's Law to above equations, the reflection coefficients can be rewritten as:

$$r_{TE} = \frac{n_1 \cos\theta_1 - \sqrt{n_2^2 - n_1^2 \sin^2\theta_1}}{n_1 \cos\theta_1 + \sqrt{n_2^2 - n_1^2 \sin^2\theta_1}}$$

$$r_{TM} = \frac{n_2^2 \cos\theta_1 - n_1 \sqrt{n_2^2 - n_1^2 \sin^2\theta_1}}{n_2^2 \cos\theta_1 + n_1 \sqrt{n_2^2 - n_1^2 \sin^2\theta_1}}$$

Once the angle of incidence exceeds the critical angle (total internal reflection)[3], the term inside square-root becomes negative. This implies that r is complex and hence a phase shift is imposed on the reflected wave:

$$R = \exp(j\phi)$$

where the phase shifts for different polarisations are given by:

$$\phi_{TE} = 2 \tan^{-1}\left(\frac{\sqrt{n_1^2 - n_2^2}}{n_1}\right)$$

$$\phi_{TM} = 2 \tan^{-1}\left(\frac{\sqrt{\frac{n_1^2}{n_2^2} n_1^2 - n_2^2}}{\frac{n_1^2}{n_2^2} n_1}\right)$$

The reflectance can also be defined through above derivation of reflection coefficient by:

$$R = \frac{E_r^2}{E_i^2} = r^2$$

Here the wavevector can be expressed in relative phase in propagation distance:

$$k = \frac{\phi}{z}$$

The further relation between wavevector and phase shift will be discussed in modes of planar waveguides to explain the propagation of waves within the waveguiding system.

5.3 Modes of Planar Waveguides

Starting with the simplest planar waveguide, Figure 5.4 shows the propagation and confinement analysis in a planar waveguide. Let the waveguide height be h, and light propagation be in the z direction. In this case, light is confined in one dimension (y-axis) by total internal reflection. The zig-zag pattern[3] in Figure 5.4 presents the propagation path within the waveguide, where the wavevector of light propagation is $k=n_1k_0$. The associated diagram in Figure 5.4b shows the two decomposed components of wavevector k in y and z directions to be:

$$k_y = n_1 k_0 \cos\theta_1$$

$$k_z = n_1 k_0 \sin\theta_1$$

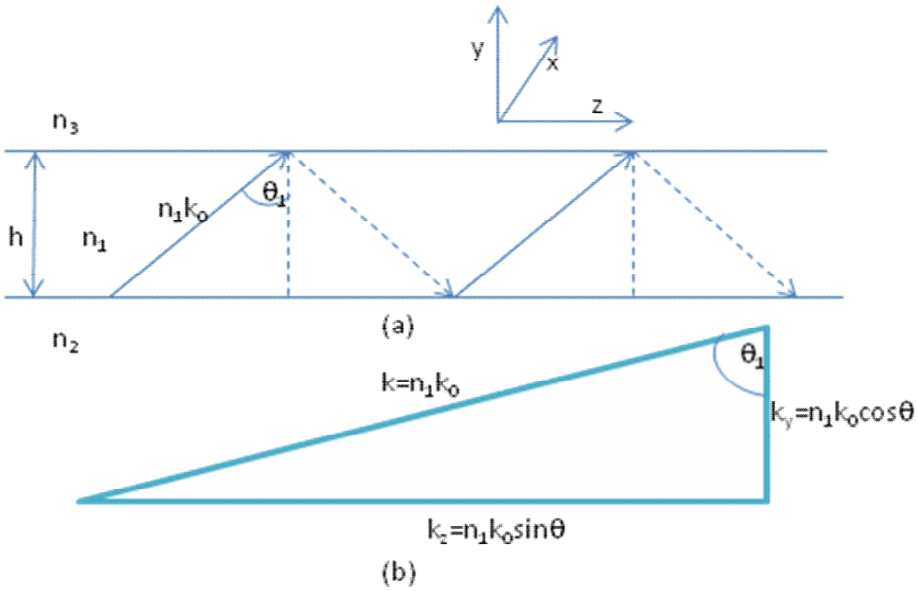


Figure 5.4: a: Propagation in a planar waveguide, b: The relationship between propagation constants.

Since the light wave will be reflected at each interface, there must be a phase shift occurring. For a planar waveguide with a thickness of h, a phase shift (a round trip by bouncing between upper and lower claddings) is represented as:

$$\Phi_h=2k_yh=2k_0n_1h\cos\theta_1$$

The total phase shift would be $\Phi_h-\Phi_u-\Phi_l$, where Φ_u is the phase shift at upper interface, and Φ_l is the phase shift at the lower interface.

$$\Phi_t=2k_0n_1h\cos\theta_1-\Phi_u-\Phi_l$$

For consistency, this total phase shift must be a multiple of 2π, hence:

$$2m\pi=2k_0n_1h\cos\theta_1-\Phi_u-\Phi_l$$

where m is an integer. This indicates that light cannot travel at all angles, but only at those discrete angles corresponding to integral values of m. Each of these allowed angles is referred to as a mode of propagation, and the mode number is the value of integer m. But there is also a limit on m, indicating that there are limited numbers of modes the waveguide can support. The limiting conditions correspond to the propagation angle θ_1, refractive index of core medium and the height of the waveguide. The modes of propagation are not interesting in the case of planar waveguides, as there is no practical application of them. Further considerations of waveguide supporting modes will be discussed in the case of 2D confined ridge waveguides.

5.3.1 Symmetrical Planar Waveguide

The definition of a symmetrical planar waveguide is to have both upper and lower claddings of the same refractive index. Therefore, the reflections from upper and lower interfaces are identical, resulting a symmetrical mode profile[3]. Identical refractive index of upper and lower cladding means that $\Phi_u = \Phi_l$(same phase shifts at upper and lower interfaces). According to the phase shift equation in TE polarisation ($\Phi_u+\Phi_l=2\Phi=$ $-1\sqrt{\quad}$), the equation of total shift can be rewritten as:

$$2m\pi=2k_0n_1h\cos\theta-$$ $-1\sqrt{\quad}$

Assume the minimum value that θ_1 can take is the critical angle[3]θ_c. This corresponds to the highest possible order mode. At $\theta_1 = \theta_c$, the phase shifts at interface become vanished. Above equation can be rearranged to:

$$k_0n_1h\cos\theta_c-m_{max}\pi=0$$

$$m_{max}=$$

Hence, the maximum number of modes that can be supported by this symmetrical planar waveguide can be evaluated with this equation.There is also an interesting characteristic of the symmetrical waveguide. The above equation always allows a solution when m=0, which indicates that the lowest order modes in TE_0 and TM_0 will always propagate, and the waveguide is never cut-off. It is exactly the opposite condition for an asymmetrical waveguide.

5.3.2 Asymmetrical Planar Waveguide

In contrast to symmetrical waveguide mentioned above, asymmetrical waveguide is a guiding medium with upper and lower cladding having different refractive index. In the case of asymmetrical waveguiding system, $n_2 \neq n_3$, thus, the eigenvalue equation for TE modes is slightly modified to be:

$$k_0 n_1 h\cos\theta_c - m_{max}\pi = \tan^{-1}\frac{\sqrt{\left(\frac{n_1}{n_2}\right)^2 - 1}}{1} + \tan^{-1}\frac{\sqrt{\left(\frac{n_1}{n_3}\right)^2 - 1}}{1}$$

because it is not possible to merge the two terms on the right hand side. Obviously, for total reflection at both waveguide boundaries, the propagating mode angle must be greater than both critical angles at upper and lower cladding. Therefore, at certain angle the waveguide will be cut off, where the total internal reflection condition is not met. In comparison, recall that a symmetrical waveguide will never be cut off.

5.4 Modes of Two-dimensional Waveguides

In common with modes of optical fibres, two–dimensional rectangular waveguide modes require two subscripts to identify them. However, it is not appropriate to use the same convention as used in optical fibres, because rectangular waveguides are not circularly symmetric[4]. Thus, Cartesian coordinates are preferred in this case in common with 1D planar waveguides.

To obtain the confinement factor of such a two-dimensional waveguide, the effective index of an optical mode plays an important role, as the waveguide geometries vary from one to another.

5.4.1 Modes of Rectangular Waveguides

In the case of slab waveguides, there is only one-dimensional optical guiding by the effective index between core and cladding materials. Hence, major part of light will propagate equally in the other two directions, where only the x direction in Figure 5.4 is the longer axis for waveguiding. Correspondingly, a second dimensional confinement is required to form a one-direction allowed propagation, in order to suppress any possible optical losses. Consequently, a stripe waveguide or called rectangular waveguide would be an ideal candidate for the guidance of light propagation. By adjusting the dimensions of the X and Y components, the transverse modes can be controlled properly. The ideal case would be to use the waveguide just above the cut-off frequency of the lowest mode but below the cut-off frequency for all the others, so that just one mode is propagated.

For a planar waveguide, we have $m_{max} = \frac{h}{\lambda} = \frac{2}{\lambda}$, indicating that the number of modes depends on the thickness of the waveguide along the y-component. In the case of stripe waveguide, there is an extra dimension that needs to be defined as $m_{max} = \frac{i}{\lambda} = \frac{2}{\lambda}$, relying on the width in x direction. In order to achieve single mode operation in a stripe waveguide, the cut-off conditions on both x and y components need to be met. Therefore, the modes of rectangular waveguides are highly depending on the dimensions of h and i. For an optical signal waveguiding at telecom wavelengths, by using the formula provided above, the single mode operation of the stripe waveguide requires h and I to be at least smaller than 750nm, which is the cut-off condition in both dimensions. To provide an extremely low-loss propagation, the sidewalls in x and y dimensions have to be nicely etched for reducing the surface roughness. Then the signal can be properly guided though the waveguide without wasting power in the excitation of higher order modes.

5.4.2 Modes of Ridge Waveguides

The single-mode stripe waveguides require extremely small dimensions (typically a few hundred nanometers) and smoothly etched sidewalls, which increase the difficulty of device process. In contrast, ridge waveguides provide relative easy process and reasonable two-dimensional optical confinement. To optimize the etch depth of ridge waveguides at a specified width (5µm) and thickness (3.5µm), simulations of cross-sectional optical modes are carried out extensively at different etch depth by FIMMWAVE (2D optical waveguide simulator).

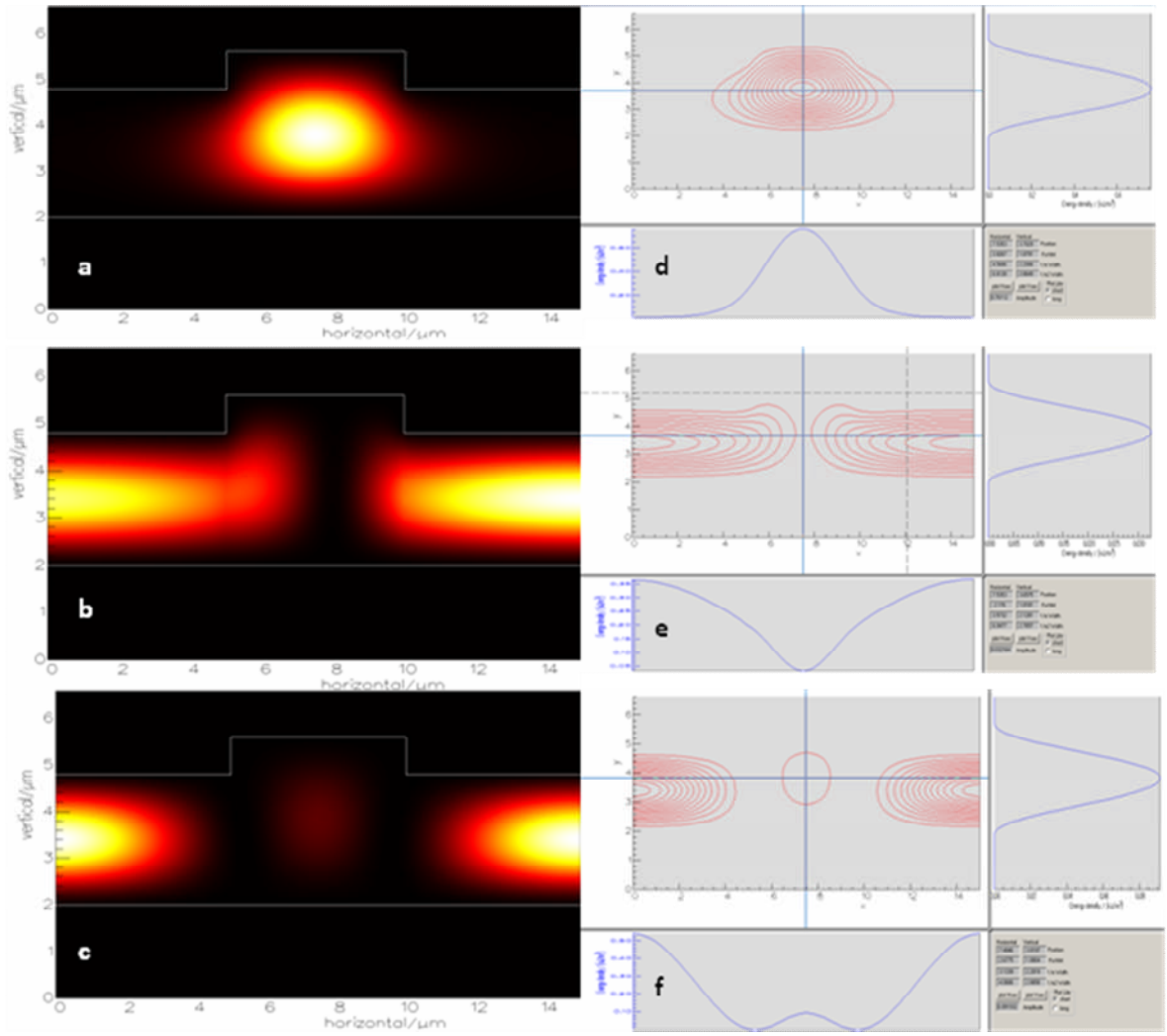


Figure 5.5: W = 5µm, t = 3.5µm, h=0.8µm; a)TE, b) and c) are the intensity plots of first three TE modes; d), e) and f) are the corresponding contour plots.

To clarify, a 5µm wide ridge waveguide is the narrowest dimension that can be achieved with optical microscope alignment using our photolithography technique. Obviously, any wider ridges would easily result the excitation of higher order transverse modes during light propagation. Starting with a shallow etch (h = 0.8), the fundamental, second order and third order modes are simulated as shown in Figure 5.5, where the fundamental TE mode is confined within the ridge (see Figure 5.5a). It can be observed in Figure 5.5b and c, that the second and third order mode can only be excited outside the ridge, hence, will not be supported by this waveguide.The images in Figure 5.5d-f are the contour plots of first three TE modes, including the field distribution of each mode. There is

no allowed transverse electromagnetic field at higher order modes within this ridge waveguide, apart from the fundamental mode.

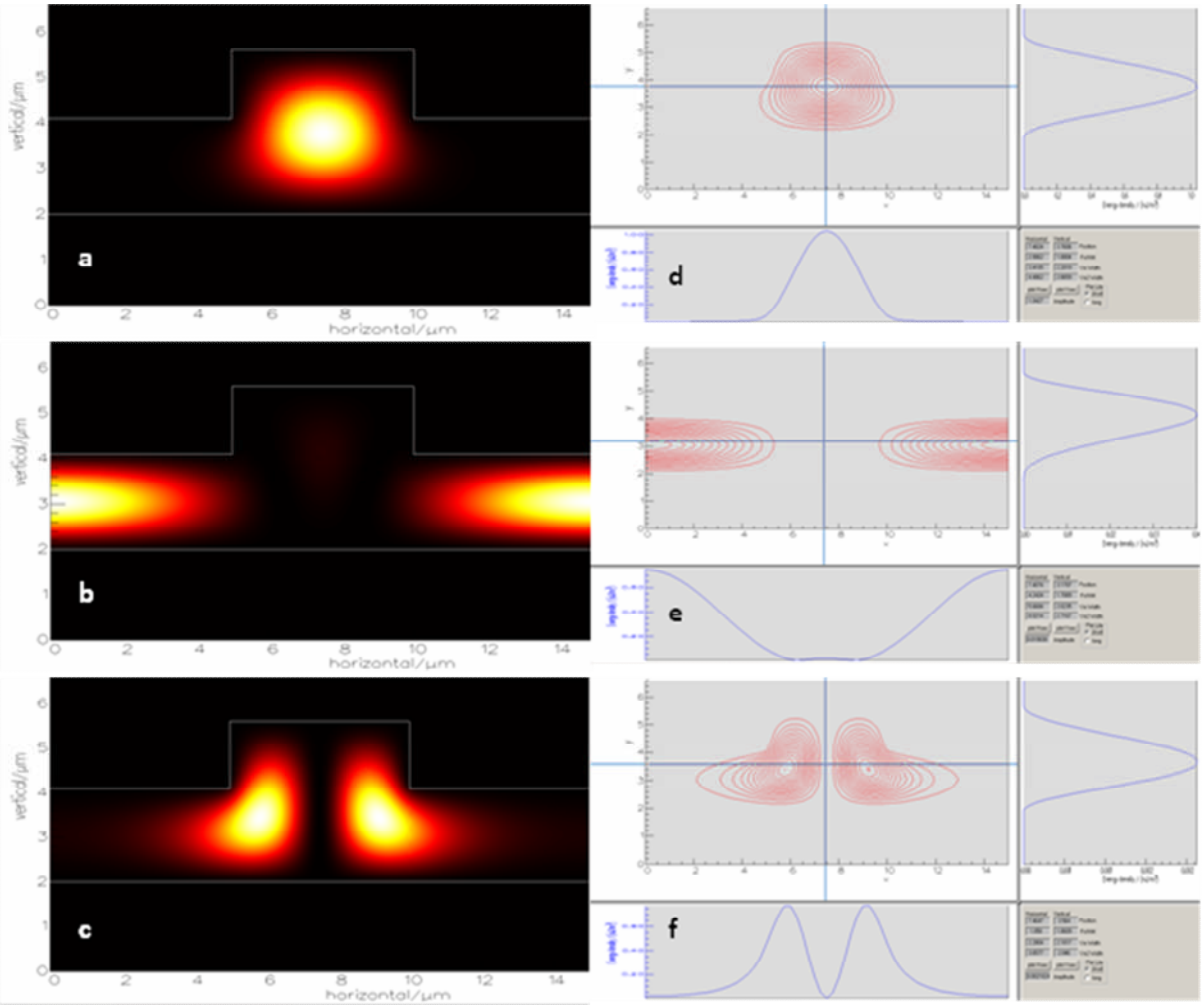


Figure 5.6: W = 5μm, t = 3.5μm, h=1.5μm; a), b) and c) are the intensity plots of first three TE modes; d), e) and f) are the corresponding contour plots.

Hence, the waveguide is operating at single mode only. If the ridge width is further increased, single mode operation will be replaced by higher mode excitation, which indicates that 5μm is the maximum ridge width supporting single mode waveguiding. As we increase the etching depth to 1.5μm, the second order mode starts to be partially supported at the edge of the ridge as shown in Figure 5.6, but the confinement of the fundamental TE appears to be much stronger.

Strong fundamental mode confinement leads to much lower optical losses in two dimensions[4], but it also brings about the excitation of a weak second order mode, which consumes some of the incident power. To solve this, by exciting the waveguide through the centre region of the ridge, the triggering of second order mode[5] can be avoided.

Therefore, a relatively strong optical confinement and single mode operation can be achieved simultaneously.

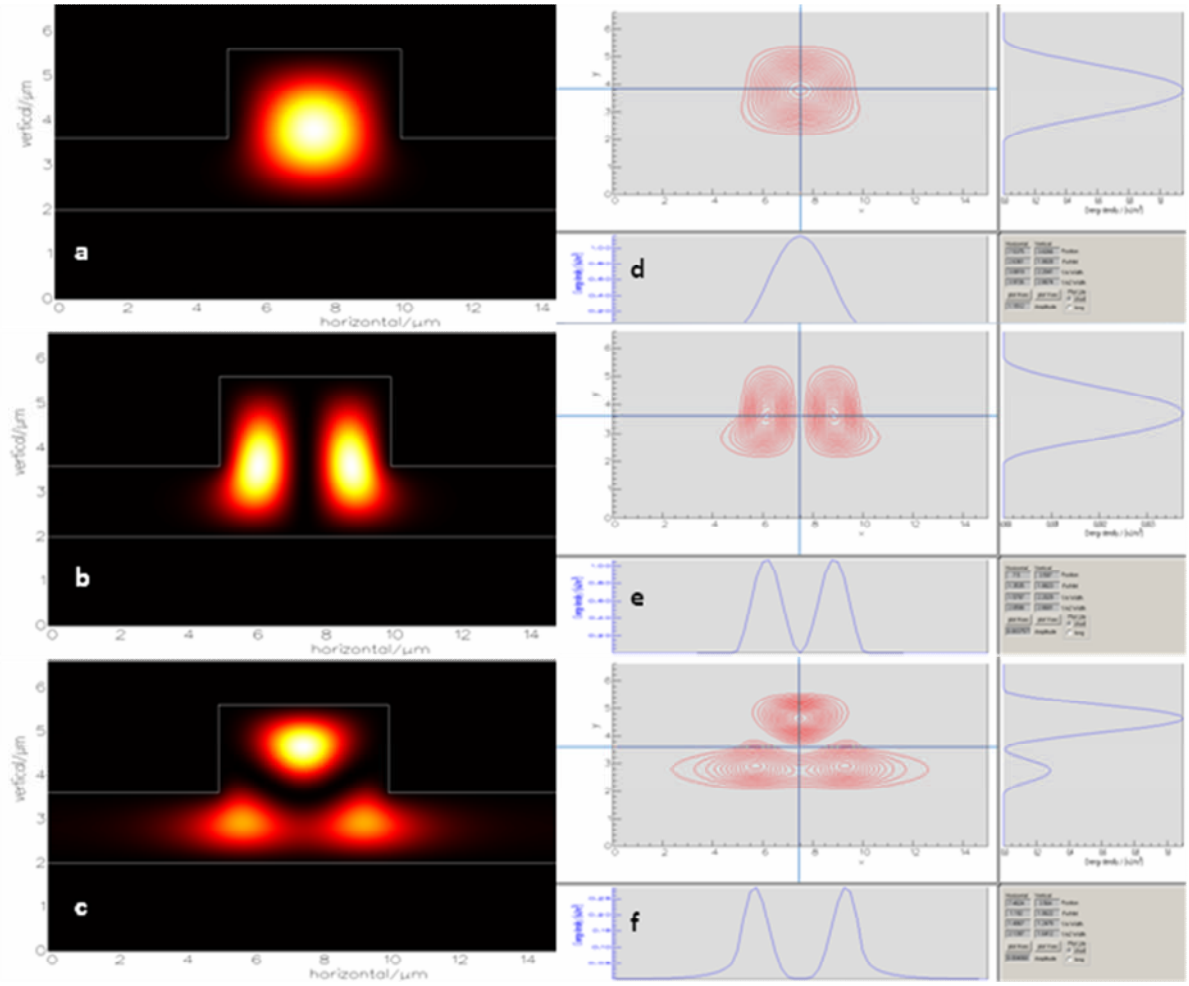


Figure 5.7: W = 5µm, t = 3.5µm, h=2µm; a), b) and c) are the intensity plots of first three TE modes; d), e) and f) are the corresponding contour plots.

Figure 5.7shows that all first three TE modes are supported by the ridge waveguide with 2µm etching depth. There is one more TE mode allowed in this waveguide in comparison with the 1.5µm etched waveguide. Hence, for long distance transmission, the major amount of incident power will dissipate due to the excitation of higher order modes[4]. In the case of passive waveguide, the ridge waveguides in Figures5.6 and 5.7 are both not good candidates for optical transmission and will not be employed due to their multi-mode operations.

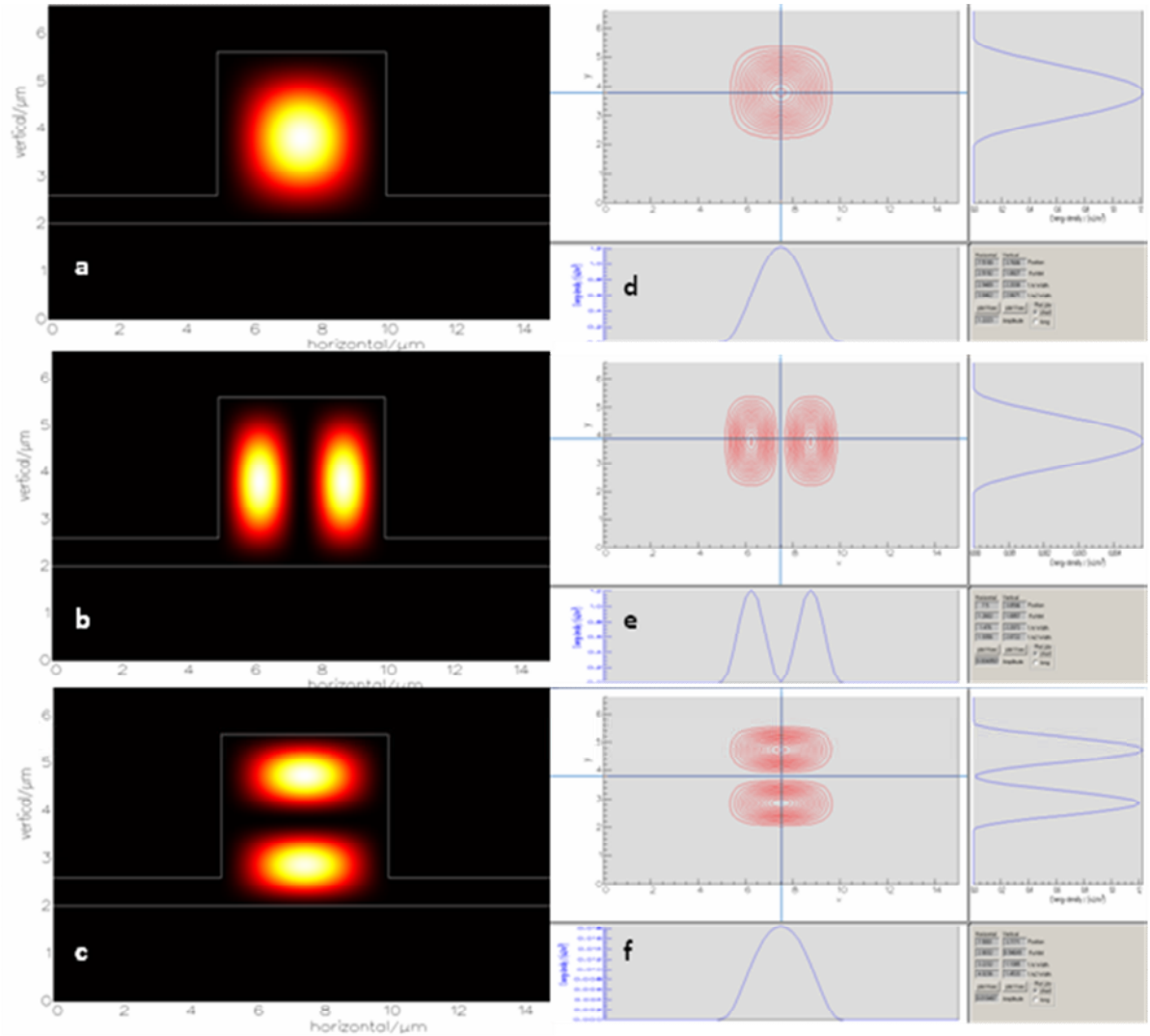


Figure 5.8: W = 5µm, t = 3.5µm, h=3µm; a), b) and c) are the intensity plots of first three TE modes; d), e) and f) are the corresponding contour plots.

But by moving to the applications of electroluminescent ridge waveguide lasers [6](active waveguides) the disadvantages of multimode operation can be suppressed, as the electrons injection profile only penetrates in the very central area of the ridge due to the position of the metal contact. Hence, the second order modes in Figure 5.6b and 5.7b will not be excited as they are close to the edge of the ridges, and the single mode operation remains.

The last simulation is based on a deep etched (3µm) rib waveguide as shown in Figure 5.8. According to the simulation results of first three TE modes, all three modes appear to be fully supported by this waveguide. Therefore, the multimode operations will be carried along in both passive and active waveguides leading to high transmission losses[5]. This

result verifies that deep etched ridge waveguide is not desirable for any waveguiding system with dimensions of a few microns.

But apart from optical losses, a deeply etched rib waveguide can also provide a better electrical confinement. Especially in the case of semiconductor lasers, injection current profile can be well controlled by the dielectric materials filled in the etched area, or even simply by the air. Therefore, there is a trade-off to be considered in deeply etched rib waveguide laser. In summary, the etch depth right above 50% of the waveguide thickness in the case of 5µm ridge width and 3.5µm ridge thickness is the optimum dimension for an active waveguiding system, enabling both strong mode confinement and single mode operation. But a further electrical confinement may be considered to increase the laser efficiency.

Due to technical limitation of device fabrication, the laser device with this optimum ridge width has not been fabricated. A relatively wider ridge laser with 50µm width and 0.8µm down-etched is fabricated.

5.5 Proposed Monolithic Integration of InAs/GaAs QD Lasers and Amorphous Si Waveguides on Si Substrates

The hybrid silicon platform is described which can be usedto integrated III–V optoelectronic components with siliconphotonics. The novelty of this approach lays in the waferscale fabrication it opens up for lasers and other activedevices on a silicon platform.

As silicon is transparent above 1.1µm, therefore, it is an ideal candidate for passive waveguiding system at telecom wavelength transmission, where the active photonic devices remain blank on silicon substrates[7].The hybrid-silicon platform allows silicon photonic devices to be integrated with active optoelectronic devicesmore commonly associated with III–V materials such as: electrically pumped lasers and modulators. In particular, the electrically pumped InAs/GaAs QD lasers fabricated in this project can be a key breakthrough for the integration of high-performance III-V lasers with silicon waveguides on silicon substrate as a multi-channel transmitter.

In this case, both passive and active photonic devices can bedemonstrated built on silicon substrate substrates such as wavelength division multiplexing(WDM) splitters for

fiber to the home applications and high speed optical modulators. The schematic of a 4-channel integrated WDM transmission[7] is shown in Figure 5.9. Four individual InAs/GaAs QD lasers on silicon substrate can be modulated separately at a modulation speed between 1-10 GHz, and subsequently coupled into the hydrogen incorporated amorphous silicon (a-Si:H) waveguides, which are multiplexed into a multimode optical fibre. To avoid the re-growth of III-V modulator on silicon, the external modulator can be replaced by the direct modulation over the QD lasers, and then butt-coupled into the a-Si:H waveguides.

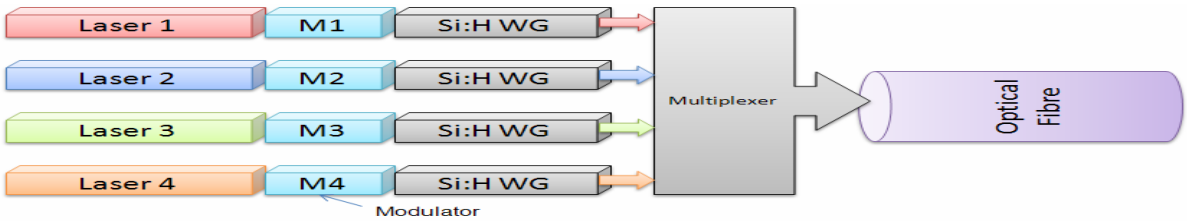


Figure 5.9: 4-channel integrated wavelength division multiplexing (WDM) transmission.

Schematic of the coupled-cavity integrated laser-waveguide system is shown in Figure 5.10. The ridge widths of the laser and waveguide are the main factor influencing to coupling efficiency. They are normally required to be the same for both laser and waveguide. In this case, a similar optical mode profile to the laser mode can be achieved. However, there are still losses arising due to the diffraction and divergence of the beam. Apart from the ridge dimensions, the next important factor causing coupling loss is the size the groove. Compared to a single cavity in which the facet reflectivity is constant for a certain wavelength, the effective reflectivity in a coupled cavity also depends on the dimensions of etched grooves, which is determined by the Fabry-Perot cavity modes formed inside grooves. Therefore, a high-quality groove with vertical and smooth side-walls is required here, which can be produced by focused-ion-beam etching[9]. In addition, the anti-reflection (AR) coating can be applied at the end of the ridge waveguide to achieve an efficient transmission.

For both active and passive devices, one of the additional parameter affecting the optical loss of the system is the dimensions of the ridge waveguides for both laser and passive waveguides. A good mode-matching between laser and passive waveguides can significantly increase the coupling efficiency, and further reduce the optical decay over the transmission within the waveguides. Thus, the transverse-mode simulation results in above sections show the optimum design of the ridge waveguides for both active and passive waveguiding systems.

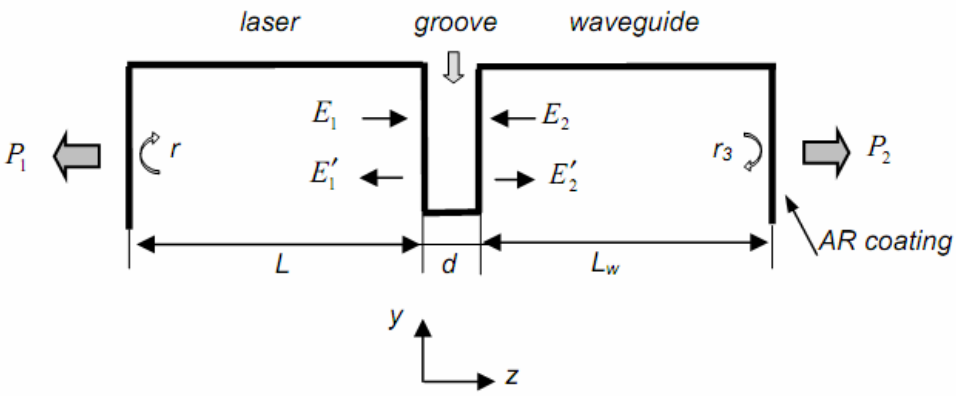


Figure 5.10: Schematic description of a laser-waveguide coupled system.

In conclusion, a groove-coupled laser/waveguide on silicon is proposed here with MBE grown InAs/GaAs QD heterostructures and focused-ion-beam etched facets for coupling. The coupling efficiency will be highly dependent on the dimensions of laser device and waveguides. From the modeling result we have obtained above, a 5µm wide, 0.8 µm shallow etched ridge appears to be the optimum dimension for the laser to efficiently couple into the waveguide with single mode operation, as deeply etched ridges tends to excite higher order transverse modes during the transmission. Therefore, the monolithically integrated laser and waveguides can be fabricated on the silicon substrate with minimum optical loss with this design.

5.6 Reference

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Chapter 6

Conclusions and Future Work

This chapter presents a summary of the work discussed in previous chapters towards the development and optimization of Si- and Ge-based InAs/GaAs quantum-dot lasers and photodetectors for silicon photonics. The achievements of this work are highlighted and conclusions that arise from this thesis are given. Finally, suggestions for future work are presented.

6.1 Summary of Present Work

The realization of semiconductor laser diodes on Si substrates would permit the creation of complex optoelectronic circuits, enabling chip-to-chip and system-to-system optical communications. Direct epitaxial growth of III-V semiconductor materials on Si or Ge is one of the most promising candidates for the fabrication of electrically pumped light sources on a Si platform. In this work we have successfully developed self-organized InAs/GaAs QD lasers directly grown on both Si and Ge substrates, with the use of the optimization of epitaxial growth, PL spectra analysis and device characterizations.

Here, we developed the first CW operated QD laser to be realized on a Ge substrate. To fabricate the laser, a single domain GaAs buffer layer was first grown

on the Ge substrate using a Ga prelayer technique, which produces an APD free GaAs buffer layer. A long wavelength InAs/GaAs QD structure was then fabricated on the high quality GaAs buffer layer. Lasing at a wavelength of 1305nm with a low threshold current density of 55.2 Acm^{-2} was observed under CW current drive at room temperature[1]. An output power of ~28mW per facet is achieved[2].

Upon the success of 1.3-µm QD laser on Ge substrate, we alsodemonstrated the first operation of an electrically pumped 1.3-µm InAs/GaAs quantum-dot laser epitaxially grown on a Si (100) substrate. The laser structure was grown directly on the Si substrate by molecular beam epitaxy. Lasing at 1.302 µm has been demonstrated with threshold current density of 725 Acm^{-2} and output power of ~26 mW for broad-area lasers with as-cleaved facets at room temperature[2]. These results are directly attributable to the optimized growth temperature of the initial GaAs nucleation layer.

The growth of InAs QD laserson group IV semiconductor substrateshas been shown to be strongly temperature dependent, with lowMigration-Enhanced Epitaxial temperatures, the material exhibiting a relatively lower defects density in comparison with high-temperature GaAs buffer layer growth. Electrically-pumped InAs/GaAs QD lasers at 1.3µm directly grown on both Ge and Si substrates have been demonstrated for the first time.

A novel dislocation reduction technique using two-dimensional strained InGaAs/GaAs superlattice as a dislocation filter was proposed, whichdemonstrates a higher efficiency of blocking TDsdue to a stronger and anisotropic strain field at theinterface of the superlattice.A Ga prelayer technique has been invented and applied to Ge substrate-based growth to achieve a significant reduction in APD density, which doesn't not work for Si substrate based epitaxial growth, with no physical explanations at the moment[1]. The As prelayer technique is replaced during the growth of GaAs buffer layer on Si substrate.

The growth temperatures of the GaAs nucleation layers on both Si and Ge substrates have been extensively studied, where 400^{o}C is found to be the optimum growth temperature in for Si substrate, and 380^{o}C for Ge substrate. At this temperature, the lowest EPDs, smallest amount of defect dots and strongest PL

intensity are achieved to suggest that the optimum laser devices can be fabricated under this condition.

The use of multiple dot layers necessitated the careful design of inter-layer barriers in order to both enhance the ability of the dots to capture carriers, and to reduce the probability of thermal evaporation of carriers out of the dots at elevated temperatures.

QD lasers grown on Ge substrates exhibited superior high temperature lasing characteristics upto 100^{o}C in pulsed mode, and 60^{o}C in CW mode.However, in the case of QD lasers on Si substrate, the laser diode suffers from substantial heat generation due to its high resistance ~18 Ohms. Therefore, the laser diode can only be operated in pulse current mode upto 42^{o}C[1]. In both cases, the laser diodes yielded a low $T_0$of 46K, as the threshold current density is extremely sensitive to temperature variations, which can be further improved by having p-doped modulation QDs.

6.2 Recent Progressand Suggestion of Future Work

In comparison with InAs QD lasers directly grown on Si, QD lasers on Ge substrates exhibit much lower threshold current density, higher output power and greater stability due to less generation of TDs and APDs. In addition, 1.3μm QD lasers on Ge substrate can be operated under CW current condition, where QD lasers on Si substrate limit to pulsed current mode due to high defect density, leading to a dramatic heat production. Therefore, InAs QD lasers on Ge shows significant advantages in device performance over QD laser directly on Si substrate, and appear to be a more realistic approach to producing commercial available high-performance QD lasers on group IV materials. However, Ge itself remains a high cost material platform for monolithic integrations.

Therefore, Ge-on-Si can be treated as a virtual substrate for the growth of top laser structures. Germanium-on-insulator-on-silicon (GeOI/Si) is reported to be the best alternative for producing 1.3μm QD laser on Si substrate, including both cost reduction and high performance. The techniques developed for 1.3μm QD laser

epitaxially grown on Ge can be directly migrated onto the GeOI/Si. GeOI/Si consists of a thin single crystal Ge layer transferred onto a Si substrate via oxide bonding. Although the surface condition and material quality of this thin Ge layer would not be as good as conventional crystalline Ge substrate, the degradation in device performance is expected to be limited to an acceptable range, as its original device performance is almost identical to QD lasers grown on GaAs. There are on-going works carrying on the growth optimization of InAs/GaAs QD laser structures on GeOI/Si substrate in UCL MBE group at the moment.

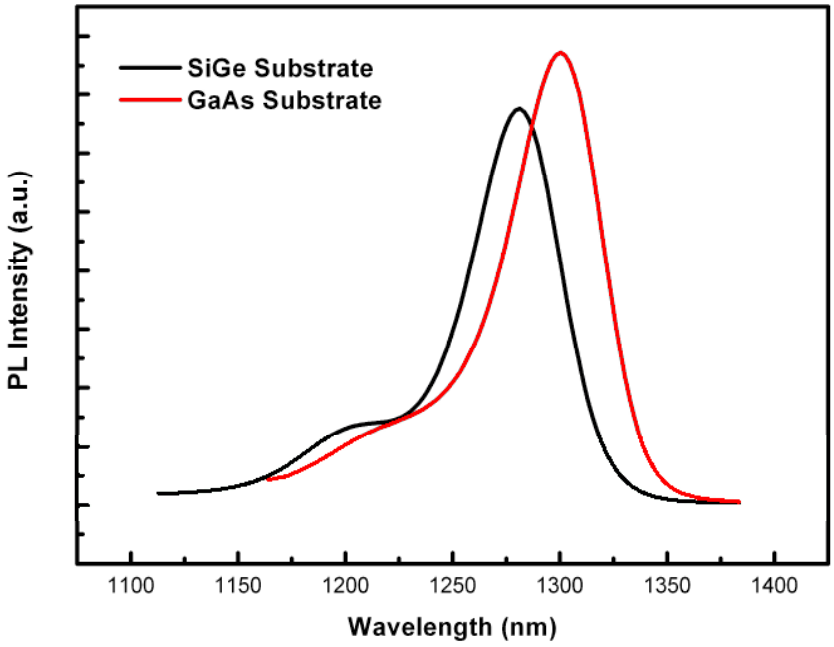

Figure 6.1: Room-temperature PL spectra of InAs QDs on GaAs and SiGe substrates.

On the other hand, as the room-temperature CW operation of InAs/GaAs QD laser has been achieved on Ge substrates, the high performance of the device indicates the potential possibilities of migrating the structure onto the well-established SiGe substrates. Therefore, an identical epitaxial structure as InAs GaAs QDs on Ge substrate was transferred onto the SiGe substrate with 6^{o}C offcut. The room-temperature PL spectra measurements were performed to compare with the reference sample on GaAs substrate, as shown in Figure 6.1. Apart from the peak of the PL being at a shorter wavelength of 1270nm, the peak PL intensity is similar to

the reference sample on GaAs. This result has further proven that the fabrication of a high-performance laser device on Ge/Si can be extremely practical. The laser device has not been processed so far, but this strong room-temperature PL is the key evidence of the future success.

In case of monolithic integration, by having our existing InAs/GaAs QD laser epitaxially grown on Si substrate, the laser can be further integrated with a waveguiding system. Amorphous Si waveguides provide more flexibility in design and fabrication compared to SOI-based waveguides. Therefore, we propose that the current laser device on Si substrate can be further processed for laser-waveguide integration on the same substrate using a lower-cost a:Si-H (hydrogen incorporated amorphous silicon) waveguides fabricated by plasma-enhanced chemical vapor deposition (PECVD).

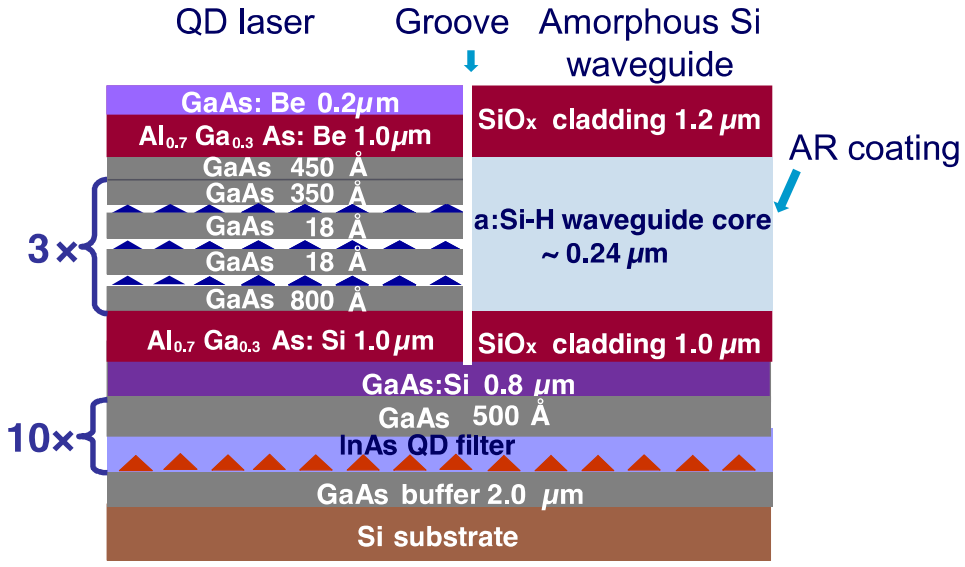

Figure 6.2: Schematic of an groove-coupled QD laser and a:Si-H waveguide on a Si substrate.

The a:Si-H waveguides exhibit an extremely low propagation loss of ~1 dB/cm in the wavelength range of 1.3-1.55 μm. This on-chip integration approach will introduce flexibility in design and fabrication, which is important for the development of silicon photonics. The schematic of proposed laser-waveguide integration on Si substrate is shown in Figure 6.2. After the expitaxial growth of laser

structures, the sample need to be patterned and dry etched, using Cl_2/Ar Inductively Coupled Plasma (ICP), to delineate the regions where the waveguide is to be deposited. The SiO_x/a:Si-H/SiO_x multimode waveguide therefore can be deposited by PECVD [3]. The critical issue here is the optical coupling between groove-coupled edge-emitting laser and the planar waveguide, which is strongly dependent on the etched facet quality and groove dimension. Instead of dry etch, focused ion beam (FIB) which is available at London center of Nanotechnology (LCN) can be utilized to create a smooth and vertical sidewall, which is almost similar to as-cleaved facet. An Al_2O_3 anti-reflection (AR) coating can be further applied at the end of the waveguide to reduce the total transmission loss within the waveguide [3].

6.3 References

[1] H. Liu, T. Wang, Q. Jiang, R. Hogg, F. Tutu, F. Pozzi, and A. Seeds, Long-wavelength InAs/GaAs quantum-dot laser diode monolithically grown on Ge substrate, Nature Photon. 5, 416 (2011).

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[4] J. Yang, P. Bhattacharya, and Z. Mi, High-performance $In_{0.5}Ga_{0.5}As$/GaAs quantum-dot laser on silicon with multi-layer quantum-dot dislocation filter, IEEE Trans. Electron Dev. 54(11), 2849-2855 (2007).

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Appendix A

Experimental Set-up for Laser Device Characterization

The performance of a laser device is judged mainly on the value, and temperature dependence, of its threshold current density, J_{th}. This can be obtained by plotting the intensity of the emitted electroluminescence (EL) as a function of the injected current.

The experimental arrangement for I-L characterization is drawn schematically in Figure A.1 A computer controlled pulsed current source was used to drive the device. A pulsed current source was used in order to minimise any heating effects originating from the injected current. Pulses of 0.1µs duration and 0.01% duty cycle were typically employed. Optical power detection was via anInGaAs photodetector. In these measurements, sample temperature is monitored by specially designed laser mount by thermal-electrical temperature control.

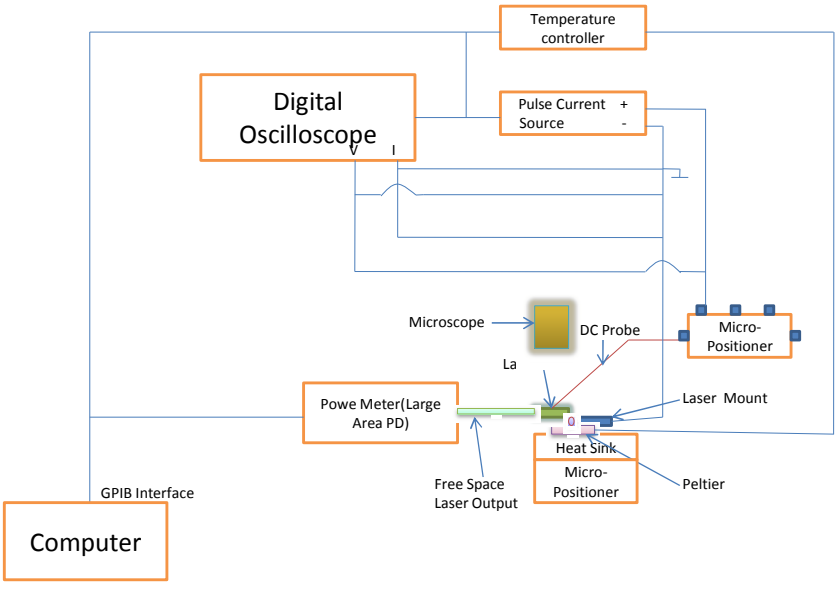
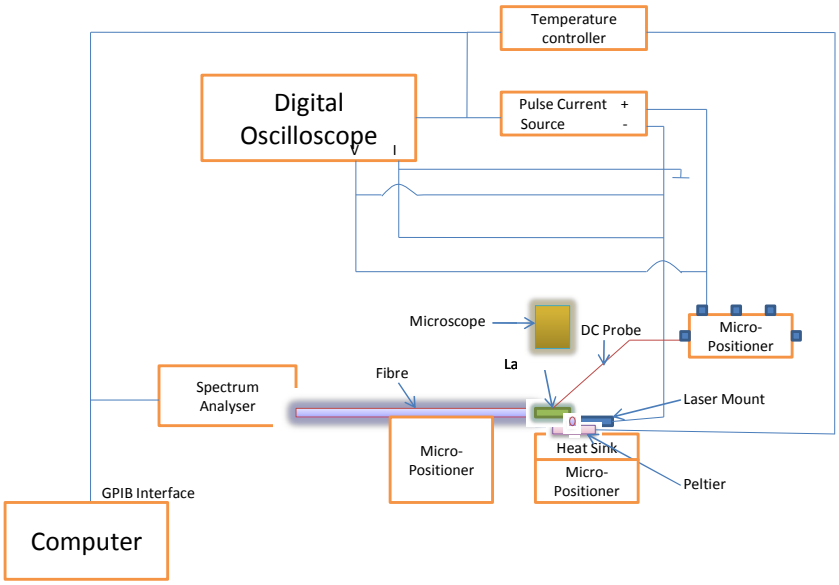


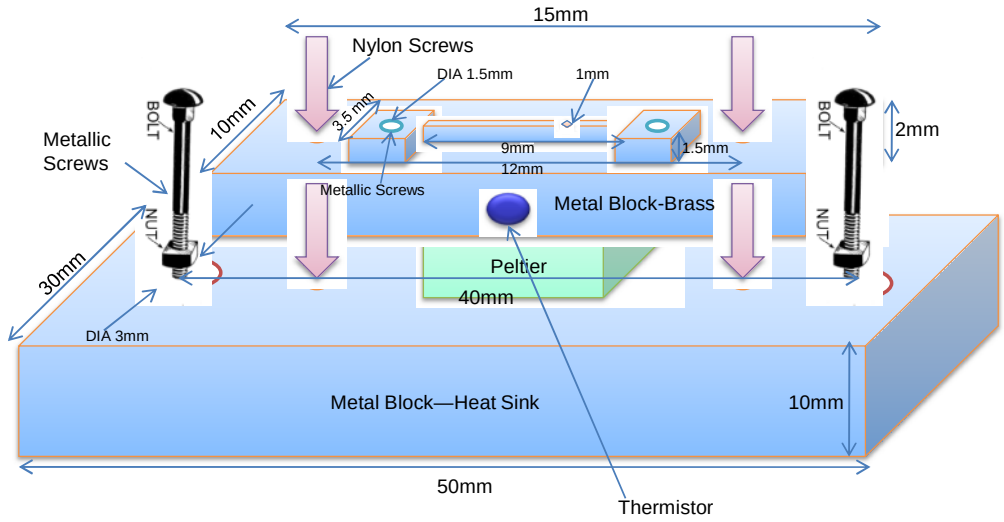
Figure A.1: Experimental arrangement for I-L measurements of laser diodes.



Setup for Spectral Characteristics (Wavelength & Linewidth Measurements)

Figure A.2: Experimental arrangement for spectral characterization of laser diodes.

Figure A.2 is the schematic diagram showing the arrangement of experimental apparatus for laser spectral characterization, which has the photodetector replaced by the spectrum analyzer. Lastly, Figure A.3 shows the design and dimension of the TE temperature controlled laser mount.



Schematic of Designed Laser Mount

Figure A.3: Schematics of designed laser mount.

Appendix B

Optimization of Ni/GeAu/Ni/Au Contact Metal

A good Ohmic contact is critical to the performance of discrete devices as well as the material quality. We have studies the effect of annealing temperature on the contact resistance of the Ni/GeAu/Ni/Au (5nm/125nm/25nm/200nm) contact metallization on N+ GaAs. The rapid thermal annealing is carried out between 380^{o}C to 460^{o}C by thermal couple readings, which is correspondent to the temperature range of 280^{o}C to 400^{o}C by pyrometer readings. Figure B.1 shows the I-V curves of Ni/GeAu/Ni/Au annealed at 327^{o}C, 360^{o}C, 380^{o}C and 400^{o}C (pyrometer reading), where the sample annealed at 280^{o}C is non-Ohmic, thus, is not shown in the plot.

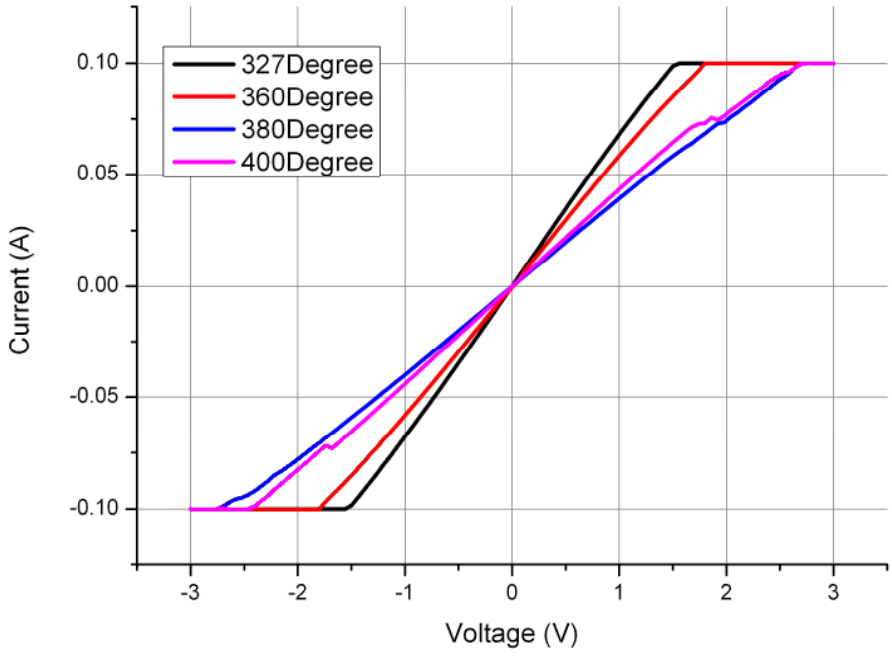


Figure B.1: I-V characteristics of Ni/GeAu/Ni/Au N+ contact metal on GaAs at different annealing temperature.

It can be clearly observed that the sample annealed at 327^{o}C has the steepest slope among all. In Figure B.2, the contact resistance variation study proves that 407^{o}C for thermocouple reading (correspondent to 327^{o}C for pyrometer) is the optimum annealing temperature to achieve a low-resistance Ohmic contact on N+ GaAs.

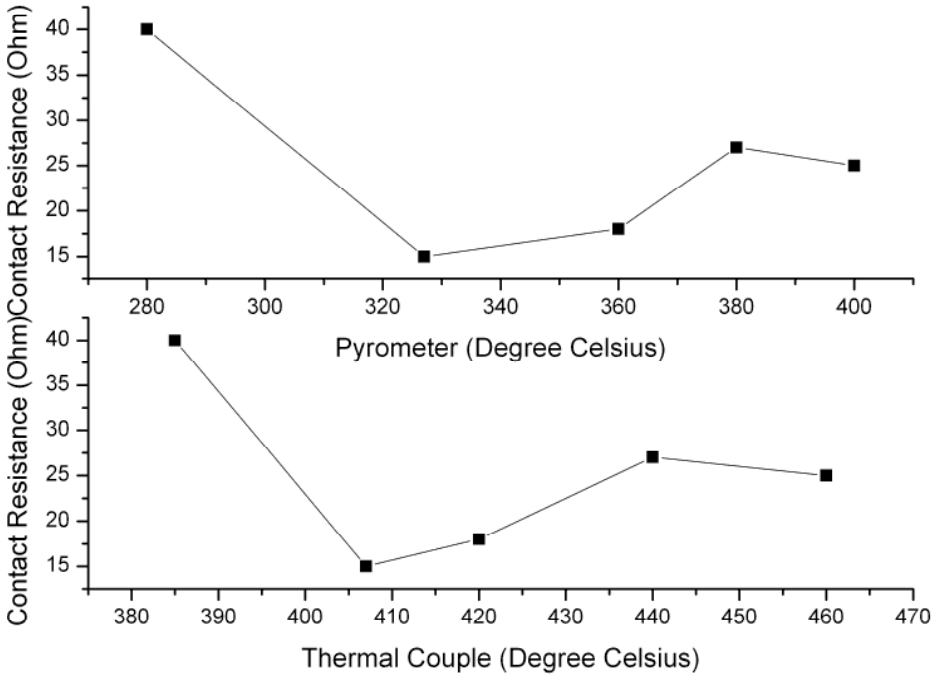


Figure B.2: Contact Resistance of Ni/GeAu/Ni/Au at different annealing temperature. Top: Pyrometer readings, Bottom: Thermocouple readings.

Appendix C

Etch Pit Density

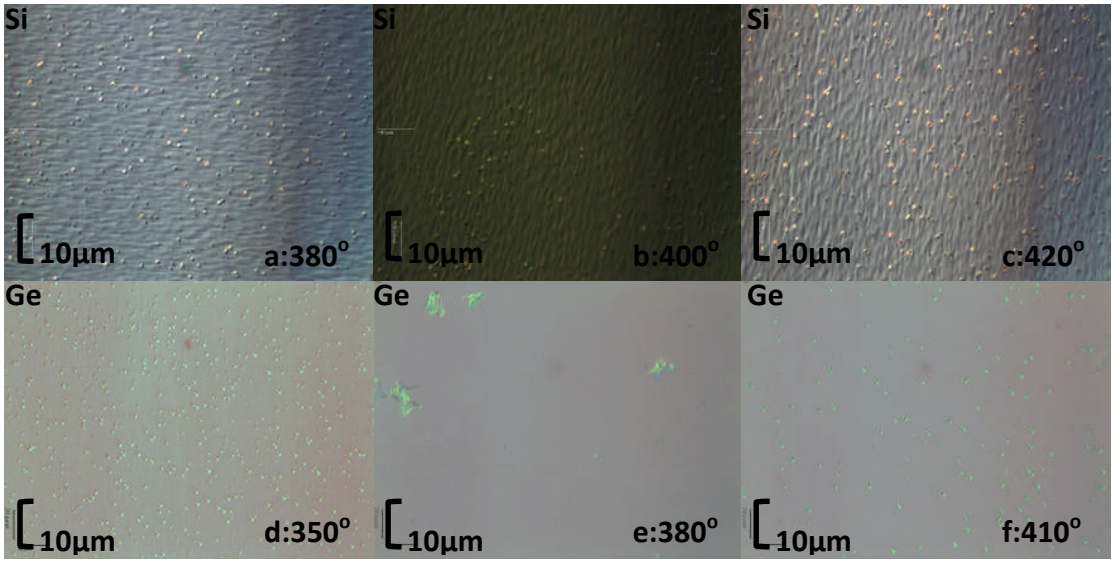


Figure C.1: Microscope images of Etch Pit Density (EPD) of InAs/GaAs QD lasers on Si and Ge substrates with different nucleation temperature. a)380°C on Si, b)400°C on Si, c)420°C on Si, d)350°C on Ge, e)380°C on Ge and f)410°C on Ge.

EPDs/Annealing Temp	380°C (Si) 350°C(Ge)	400°C (Si) 380°C(Ge)	420°C (Si) 410°C(Ge)
Si Substrate	$1.03\times10^{7}cm^{-2}$	$6.03\times10^{6}cm^{-2}$	$8.17\times10^{7}cm^{-2}$
Ge Substrate	$1.7\times10^{7}cm^{-2}$	$8.0\times10^{5}cm^{-2}$	$3.7\times10^{6}cm^{-2}$

Table C.1: Summary of EPDs of InAs/GaAs QD lasers on Si and Ge substrates with different nucleation temperature.

Appendix D

Oxide Stripe Laser Process

Oxide Deposition:

1. Clean samples: Acetone/Methanol/IPA/Dry N_2
2. Deposit 200nm PECVD SiO_2:
   340kHz, 550mTorr, 300^oC, 60W, 120sec, SiH_4
3. Clean samples: Acetone/Methanol/IPA/Dry N_2

Photolithography (Top-contact Window Definition):

4. Dehydration: Bake 150^oC 5mins
5. Spin Resist: Shipley 1818
   Dispense 5sec 500rpm
   Spin 30sec 4000rpm
6. Post Bake: 115^oC 1min
7. Mask Aligner: 5sec exposure (Mask 3—20um Stripes)
8. Development: MF319 Developer 45sec

Oxide Etch:

9. Etch Prebake: 127^oC 7mins (Hardening the resist)
10. HF wet etch 78sec (127^oC post bake is required to protect photoresist to be attacked by acid)
11. Clean samples: Acetone/Methanol/IPA/Dry N_2

Photolithography (Top-Contact Definition for Liftoff):

Method 1: Chlorine Benzene Soaking

12. Dehydration: Bake 150^oC 5mins
13. Spin Resist: Shipley 1818
    Dispense 5sec 500rpm
    Spin 30sec 4000rpm
14. Post Bake: 115^oC 1min
15. Mask Aligner: 5sec exposure (Mask 3—50um Stripes)
16. Chlorine Benzene Soaking: 10mins
17. Chlorine Benzene Bake: 90^oC 5mins
18. Development: MF319 Developer 60sec

Method 2: LOR/S1805 Double Layers

19. Dehydration: Bake 150^oC 5mins
20. Spin Resist: LOR 10B

Dispense 5sec 500rpm
Spin 30sec 4000rpm

21. Post Bake: 190°C 10mins
22. Spin Resist: Shipley 1805
    Dispense 5 sec 500rpm
    Spin 30sec 4000rpm
23. Post Bake: 115°C 1min
24. Mask Aligner: 2sec exposure (Mask 3—50um Stripes)
25. Development: MF319 Developer 45sec

Top-contact Metal Deposition:

26. De-oxidation: Dip in HCL:H_2O(1:1) 5sec
27. Thermal Evaporator: **Si Substrate (N+)** - Evaporate Ti/Au (5/200nm) for P-contact, **Ge Substrate (P+)** - Evaporate Ni/GeAu/Ni/Au (5/125/25/200nm) for N-contact
28. Liftoff metal: Acetone Soaking — aggressive acetone spray aids in liftoff
29. Clean samples: Acetone/Methanol/IPA/Dry N_2

Bottom-contact Process:

30. Thinning: Thin the wafer backside to ≈150um
31. De-oxidation: Dip in HCL:H_2O(1:1) 5sec
32. Thermal Evaporator: **Si Substrate (N+)** - Evaporate Cr/Au (20/200nm) for N-contact, **Ge Substrate (P+)** - Evaporate Au/Zn/Au (50/25/200nm) for N-contact
33. Rapid Thermal Annealing Metal Contacts for 30sec
34. Cleave sample into desired cavity lengths

Appendix E

Ridge-waveguide Laser Process

Oxide Deposition:

1. Clean samples: Acetone/Methanol/IPA/Dry N_2
2. Deposit 200nm PECVD SiO_2:
   340kHz, 550mTorr, 300°C, 60W, 120sec, SiH_4
3. Clean samples: Acetone/Methanol/IPA/Dry N_2

Photolithography (Ridge Definition):

4. Dehydration: Bake 150°C 5mins
5. Spin Resist: Shipley 1818
   Dispense 5 sec 500rpm
   Spin 30sec 4000rpm
6. Post Bake: 115°C 1min
7. Mask Aligner: 5sec exposure (New Mask — 20um Ridges)
8. Development: MF319 Developer 45sec

Oxide Reactive Ion Etch (Transfers photoresist soft mask to oxide hard mask):

9. Etch oxide in Oxford OPT Plasma RIE etcher:
   Conditioning: CHF_3 30sccm, O_2 5sccm, 100W, 35mTorr
   Oxide Dry Etch: CHF_3 30sccm, O_2 5sccm, 100W, 35mTorr
10. Alternatively dip in BHF(Buffered HF)
    HF:NH_4F = 1:6 78sec
11. Remove Resist: Photoresist stripper or Ashing

GaAs Mesa Etch (Etch active waveguide in semiconductor):

12. Etch GaAs in STS ICP(Inductively-Coupled Plasma) etcher:
    GaAs Dry Etch: $SiCl_4$ 7sccm, Ar_2 20sccm, 250W
    Inspect etch depth with laser based surface profiler
13. Alternatively etch GaAs by using III-V universal etchant(Adachi etch)
    Analar Potassium Dichromate: Analar Acetic Acids: Analar Hydrobromic Acid = 1:1:1
    30sec dipping
14. Remove Oxide: HF wet etch (stop when surface become hydrophobic)

Oxide Deposition:

15. Clean samples: Acetone/Methanol/IPA/Dry N_2

16. Deposit 200nm PECVD SiO_2:
    340kHz, 550mTorr, 300°C, 60W, 180sec, SiH_4 12sccm, N_2O 1420sccm, N_2 392sccm
17. Ellipsometer: Measure the approximate thickness of SiO_2 deposited
18. Clean samples: Acetone/Methanol/IPA/Dry N_2

Photolithography (P-Contact Window Definition):

19. Dehydration: Bake 150°C 5mins
20. Spin Resist: Shipley 1818
    Dispense 5 sec 500rpm
    Spin 30sec 4000rpm
21. Post Bake: 115°C 1min
22. Mask Aligner: 5secs exposure (New Mask — 10um Contact Windows)
23. Development: MF319 Developer 45sec

Oxide Reactive Ion Etch (Transfers photoresist soft mask to oxide hard mask):

24. Etch oxide in Oxford OPT Plasmon RIE etcher:
    Conditioning: CHF_3 35sccm, 100W, 35mTorr, 5mins
    Oxide Etch: CHF_3 35sccm, 100W, 35mTorr, 10mins
25. Dektak: Measure the depth of etch step(make sure no SiO_2 residues left in the etched trenches)
26. Remove Resist: Photoresist stripper or Ashing

Photolithography (P-Contact Definition for Liftoff)

Method 1: Chlorine Benzene Soaking

27. Dehydration: Bake 150°C 5mins
28. Spin Resist: Shipley 1818
    Dispense 5 sec 500rpm
    Spin 30sec 4000rpm
29. Post Bake: 115°C 1min
30. Mask Aligner: 5sec exposure (Mask 3—60um Stripes)
31. Chlorine Benzene Soaking: 10mins
32. Chlorine Benzene Bake: 90°C 5mins
33. Development: MF319 Developer 60sec

Method 2: LOR/S1805 Double Layers

34. Dehydration: Bake 150°C 5mins
35. Spin Resist: LOR 10B
    Dispense 5 sec 500rpm
    Spin 30 sec 4000rpm
36. Post Bake: 190°C 10mins
37. Spin Resist: Shipley 1805
    Dispense 5 sec 500rpm

Spin 30sec 4000rpm

38. Post Bake: 115^{o}C 1min
39. Mask Aligner: 2sec exposure (Mask 3—60um Stripes)
40. Development: MF319 Developer 45sec

P-contact Metal Deposition:

41. De-oxidation: Dip in HCL:H_2O(1:1) 5sec
42. Thermal Evaporator: Evaporate Ti/Au (5/200nm)
43. Liftoff metal: Acetone Soaking — aggressive acetone spray aids in liftoff
44. Clean samples: Acetone/Methanol/IPA/Dry N_2

N-contact Process:

45. Thinning: Thin the wafer backside to ≈150um
46. De-oxidation: Dip in HCL:H_2O(1:1) 5sec
47. Thermal Evaporator: Evaporate Ni/GeAu/Ni/Au (5/125/25/200nm)
48. Rapid Thermal Annealing Metal Contacts for 30sec
49. Cleave sample into desire cavity length